Characterization and modeling of phase-change memories

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Characterization and Modeling of Phase-Change Memories

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To my beloved uncle Antonio Marasti,
for his honesty, goodness of heart and kindness,
for his unlimited generosity,
for his positive attitude towards life,
and for all the serenity he has always given to me.

Vita brevis, ars longa, occasio praeceps, experimentum pericolusum, iudicium difficile

Hyppocrates of Klos, (ca. 460 BC – ca. 370 BC)

Contents

Introduction

Non-volatile Memory (NVM) technologies play a fundamental role in the microelectronics industry. The non-stop increasing of functionalities and performances of consumer electronic products such as digital cameras, MP3 players, smart-phones, personal computers, and, more recently, solid-state hard disks, claims for a continuous improvement of memory capacity and features.

Floating-gate-based NVMs, usually named Flash memories, represent the today mainstream in the NVM market, and are expected to be the reference technology also in the near future. Nevertheless, Flash paradigm presents intrinsic physical constraints that hamper their further scaling. In this context, there is a growing interest for alternatives, based on new materials and concepts, to go beyond Flash, the goal being increasing the memory performances, and, in the same time, reducing cost per bit and decreasing energy and power consumption.

Up to today, more than 30 *emerging* NVM technologies are have been competing to enter in the fast growing NVM market. Among these, one of the more interesting is the Phase-Change Memory (PCM).

PCM relies in the property of special materials, i.e. the chalcogenide alloys, to exist in two stable states of the matter, which have different electrical resistivities (i.e., a high-resistance amorphous phase and a low-resistance crystalline state). Phase transition is a reversible phenomenon, and is achieved by stimulating the cell with suitable electrical pulses that appropriately heat the material, triggering the phase-change. Despite the discovery of phase-change materials suitable to be integrated in semiconductor memories dates back to the '70s, the development of viable PCM prototypes has been demonstrated only recently. Today's PCM is the result of the employment of new, faster, phase-change materials, and of manufacturing expertise acquired in more than 10 years of industrial activity.

PCMs have the potentiality to improve the performances compared to Flash, featuring

faster program, better endurance, and, most of all, much higher scaling potential. For some applications, PCM can also competes with DRAM, featuring lower (but still very high) programming speed, but presenting the big advantage of being a non-volatile technology.
However, even if very promising, PCM needs to increase its cost-competitiveness compared to Flash NAND and DRAM. Moreover, the possibility of developing new interesting applications PCM-based has not been thoroughly demonstrated yet. Both aspects strongly motivate further scientific research.
The main objectives of today PCM developers are the reduction of the current needed to switch the cell in the amorphous phase, to increase memory density and decrease power and energy consumption. Another important aspect is the improvement of data retention performances to address embedded memory applications. Then, a key aspect for PCM success is, as obvious, the development of reliable and well-controlled manufacturing processes. Research on new cell architectures and new phase-change materials is needed to accomplish such ambitious goals.
This Ph.D. thesis, entirely devoted to PCM, fits in this framework. One of the main goal and *fil rouge* of this research work has been the investigation of three of the key aspects of advanced solid-state memory technology development: (a) investigation of new materials (addressed in Chapter 1), (b) advanced electrical characterization techniques (Chapter 2) and (c) modeling for comprehension of physical phenomena (Chapter 3).
The manuscript is organized as follows. After a brief introduction on PCM technology (Chapter 1), a characterization study on phase-change devices integrating carbon-doped GeTe active material is presented for the first time. Carbon-doped GeTe promises to alleviate both of the above mentioned main PCM issues, namely programming current reduction and data retention amelioration. Then, Chapter 3 shows the implementation, characterization and modeling of a low-frequency noise measurement setup. Low-frequency noise is considered one of the more sophisticated technique to investigate bulk material and interface properties, directly related to technology maturity and reliability. Finally, in Chapter 4, the $I - V$ behavior of crystalline PCM cells is investigated. Modeling of physics of PCM can indeed enable cell and material design, multilevel capabilities, as well as system design strategies (e.g. developing of read-window-of-budget tools) and scaling predictions.
The manuscript has been thought to have modularity property, that is, each Chapter is self-consistent and can be read independently. For this reason, detailed introductions with related bibliographic reference are provided at the beginning of each new topic.

Chapter 1

Elements of the Phase-Change Memory technology

1.1 Abstract

In this Chapter, fundamental aspects and properties of the Phase-Change Memory (PCM) technology are introduced. The goal of this Chapter is not to provide a complete review on the PCM subject, but introduce and clarify the minimum number of concepts and definitions helpful for the reader to tackle the following chapter of the thesis, where novel and original contributions of the author to the field of Phase-Change Memory are reported[1].

In Section 1.2, we start briefly discussing the technological context of today Non-Volatile-Memory (NVM) industry, focusing on the Flash mainstream scaling issues. Then, we introduce the physical principles in which the PCM technology relies and its most important attributes. Possible PCM applications are also discussed.

Some of the basic memory cell operations and characteristics (i.e Ovonic threshold switching, programming and reliability) are addressed in Section 1.3.

Section 1.4 is devoted to the analysis of the electrical behavior of PCM cells based on the GeTe active material. GeTe is a chalcogenide alloy that appears to be a good alternative to the today PCM reference material: the $Ge_2Sb_2Te_5$ (GST) alloy. In Chapter 2 we illustrate, for the first time, an experimental study carried out on PCM devices integrating a doped version of the GeTe material developed at CEA-Leti: Carbon doped-GeTe, showing superior performance in terms of data retention and programming

[1] For the interested reader, exhaustive reviews on the Phase-Change Memory technology published in the technical literature are listed in the bibliography [RaoWut]-[Ter09].

current reduction.
Introductory Sections 1.2,1.2.2,1.3 are strongly inspired by the review presented by [Lac08] and [Bez09]. Section 1.4 shows the results published in the paper [Per10].

1.2 Introduction

1.2.1 Technological context: Flash issues

The key driver of the Non-Volatile-Memory technologies widespread in the last 15-20 years has been the Flash memory. Scaling of the Flash NOR, used mainly for code storage, has followed the Moore's Law, featuring a cell area of 10–12 F^2, where F is the technology minimum size. The Flash NAND, which is optimized for data storage, has been even more aggressively scaled and, nowadays, has a cell size of about 4.5 F^2 [Lac08]. However, further scaling of both NOR and NAND is projected to slow down in the future, because of critical physical phenomena due to size reduction that impacts data retention performance, namely the use of thinner tunnel oxides for NOR, and electrostatic interactions issues between adjacent cells for NAND [Lai08]. Moreover, with the downscaling, the number of electrons stored in the floating gate and flowing in the device channel decreases. For this reason, since a reduced number of electrons are involved in the electronic processes of the cell, effects like the random telegraph noise occurring from trapping-detrapping phenomena cause threshold voltage instabilities and reading errors [Kur06]. For all these reasons, originated by fundamental physical limitations of the charge storage paradigm, industry is searching for alternatives to the Flash concept. Novel memory strategies have been explored in the last years both by industry and by research centers all over the world: they include Ferroelectric RAM, Magnetic RAM, and resistive memories (Phase-Change Memory, Oxide-based RAM and Solid-State Electrolyte Memory) [Bur08]. Among these, the Phase-Change memory (PCM) technology, based on the reversible phase transformation capability of special alloys named *chalcogenides*, appears to be particularly promising [Bez09].

1.2.2 Phase-Change Memory: introduction

Phase-Change Memory devices employ chalcogenide alloys. Chalcogenides are semiconducting glasses made of elements of the VI group of the periodic table, such as sulfur, selenium and tellurium. First investigations on the electrical properties of the chalcogenide materials date back to the pioneering research by S.R. Ovshinsky in the

late 1960's [Ovs68]. The concept of a non-volatile PCM, based on the properties of the chalcogenide alloys, came out at the beginning of 1970's [Nea70]. In these devices, the memory element is basically a variable resistor made of a chalcogenide material. Depending on whether the chalcogenide layer is the amorphous or crystalline state, the device resistance is high (RESET state) or low (SET state). Programming of the phase state is accomplished by current-induced Joule heating: the RESET state is achieved with a large current pulse, raising the chalcogenide temperature above the melting point. The melt chalcogenide then quenches into the glass state along the abrupt fall of the reset pulse. The SET state is recovered with a smaller current, heating the glass above the crystallization temperature and activating nucleation and growth of the crystalline phase [Iel04]. Although the inherent simplicity of the PCM concept and its compatibility with standard CMOS process, difficulties in reducing the long switching times required to program prototype devices hampered their initial development. However, the identification of new, better, phase-change materials in recent years has led to substantial improvements in the speed of PCM [Wut04]. Today, the most known and used chalcogenide material is $Ge_2Sb_2Te_5$ (GST), but many others are under investigation (doped GST and GeTe-based alloys in particular, but also many others). Since early 2000, different semiconductor industries have considered the exploitation of the PCM concept for large-size solid state memories. Compared to the Flash mainstream, the PCM technology features potential of better scalability (up to few nanometers) [Rao08], faster programming time (in the order of few nanoseconds) [Bru09] and an ameliorated endurance (up to 10^9 programming cycles) [Oh06]. Furthermore, PCM allows direct write of the memory, without the need of a pre-writing erasing step (this property is frequently named *bit alterability*). Recently, some PCM-based memory chips have already been presented in order to showcase the viability of high density standalone PCM memories from the industrial point of view: a 60-nm 512-Mb by Samsung [Oh06] and a 45-nm 1-Gb [Ser09] by Numonyx (now Micron) PCM technology have been realized. Interestingly, PCM technology comprehends features of both NVM and DRAM (see Table 1.1 [Bez09]). Among others, very important for the application point of view are PCM properties of non-volatility, exploited to reduce power, and direct write, enabling the use of PCM like DRAM. For these reasons, PCM could cover a broad range of possible applications. In particular, PCM can address wireless systems, embedded applications, solid state storage subsystems and computing platforms [Bez09].

Attributes	PCM	EEPROM	NOR	NAND	DRAM
Non-volatile	Yes	Yes	Yes	Yes	No
Scaling to	sub-2x nm	n.a.	3x nm	2x nm	3x nm
Granularity	Small/Byte	Small/Byte	Large	Large	Small/Byte
Erase	No	No	Yes	Yes	No
Software	Easy	Easy	Moderate	Hard	Easy
Power	$\sim$ Flash	$\sim$ Flash	$\sim$ Flash	$\sim$ Flash	High
Write bandwidth	1-15+ MB/s	13-30 KB/s	0.5-2 MB/s	10+ MB/s	100+ MB/s
Read latency	50-100 ns	200 ns	70-100 ns	15-50 μs	20-80 ns
Endurance	10^{8+}	10^5-10^8	10^5	10^{4-5}	Unlimited

Table 1.1: Comparison of key attributes among PCM, floating-gate NVM (EEPROM, NOR and NAND Flash) and DRAM [Bez09].

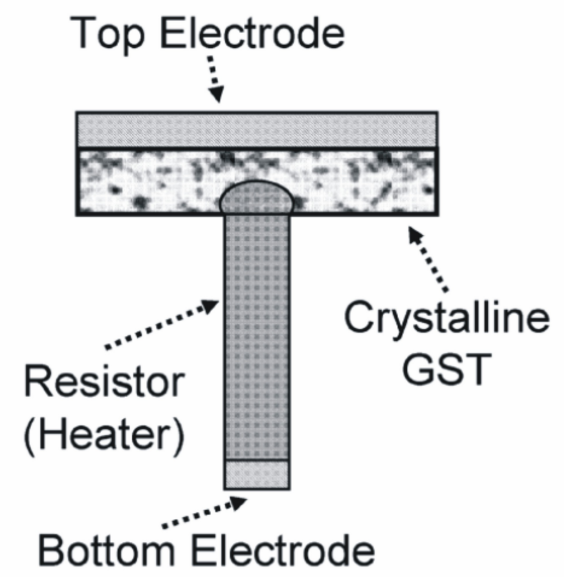


Figure 1.1: Lance-type PCM cell. The current concentration at the heater-GST interface results in local heating of the GST in a hemispherical volume [RaoWut].

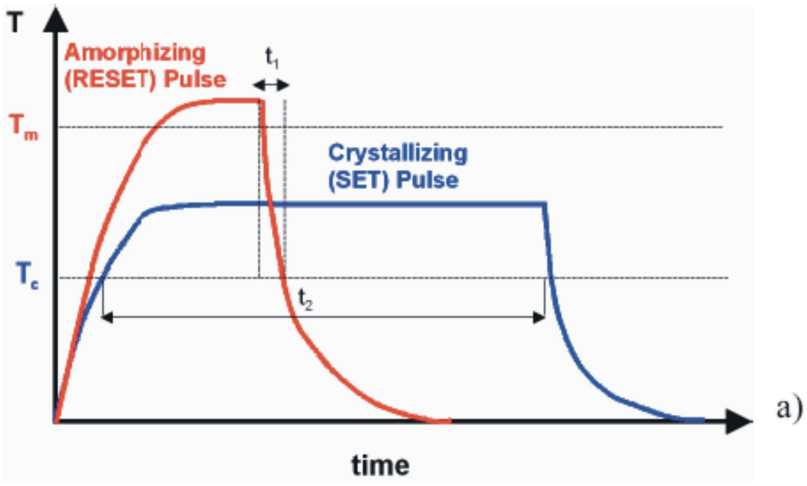
1.3 Phase-Change Memory: basic memory operations

1.3.1 PCM lance cell

The schematic of a common PCM device structure (the *lance* device) is shown in Figure 1.1. The active phase-change material (GST, in the example in the figure), is sandwiched between a top metal contact and a resistive plug, also called heater. In these cells, when a suitable electrical pulse is applied, current crowding at the heater/GST interface leads to joule heating of a mushroom-shaped volume of the phase-change material, which changes its state. As already said, when the phase-change material is in its crystalline low-resistive form, the overall device resistance is low (corresponding to a logic 1, or SET). On the other hand, amorphization of this area hampers subsequent current flowing and result in a overall high cell resistance (corresponding to a logic 0, or RESET) [Lac08]. Figure 1.2 shows typical programming pulses (a), and I-V characteristics of a PCM cell (b). In figure 1.2(a) the temperature evolution in the GST region near the heater interface as a results of the current pulses is displayed. To form the amorphous mushroom region, a tenths of nanosecond range current pulse heats up the region until GST reaches the melting temperature (around 620 °C). Then, the following cooling, along the falling edge of the current pulse, freezes the molten material into a disordered amorphous phase. To recover the crystalline phase, another current pulse, with a duration (for GST-based technology) in the range of hundred of nanoseconds, but with a lower amplitude, heats the cell again resulting in temperatures above the crystallization temperature (associated to the given current pulse duration) but below the melting temperature. In this way, the spontaneous amorphous-to-crystalline transition is speeded-up and crystallization by nucleation and growth processes occurs [Lac08b].

1.3.2 Ovonic Threshold Switching

Figure 1.2(b) shows the typical I-V curve of a cell for both states. Since the electrical resistivity of the two phases differs by orders of magnitude, reading is accomplished by biasing the cell and sensing the current flowing through it. Note that the I-V behavior of the RESET state is very different from the quasi-linear behavior of the SET state. As the bias reaches a certain voltage (the threshold switching voltage, V_{TH}) a *snapback* takes place and the conductance abruptly switches to a high conductive state [Lac08b]. On the other hand, the I-V curve of the crystalline material does not feature threshold switching and approaches the I-V of the amorphous state in the high current zone. The occurrence of this so-called *Ovonic threshold switching* is a very important characteristic of phase-



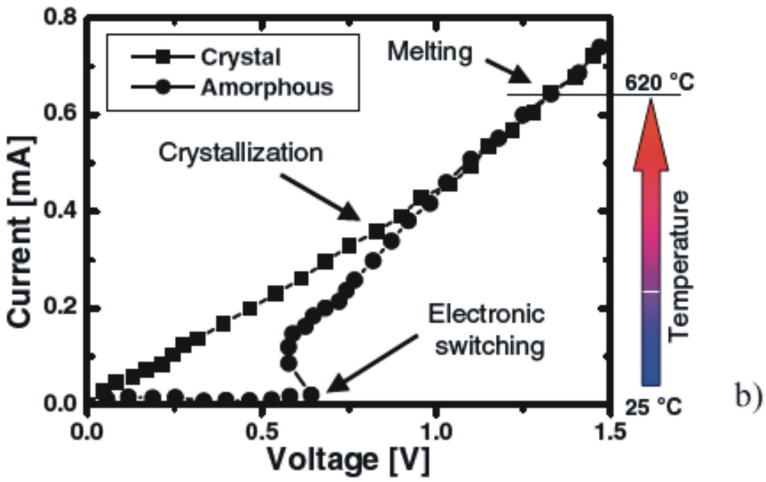


Figure 1.2: (a) Thermal-induced switching of the phase-change material, either by melting and subsequent quenching in the amorphous phase (RESET pulse), or by heating in the solid state inducing crystallization of the amorphous state (SET pulse) [Lai01][Lac08]. (b) I-V curves of both the crystalline and amorphous state. The high current levels required for the Joule-heating can be obtained at low voltages even for the amorphous state thanks to the Ovonic threshold switching phenomenon [Lac06][Lac08].

change material. Without such a switching mechanism, that allows large currents to flow in the amorphous material at low voltages ($\sim$ few Volts), very high voltages ($\sim$ 100 V) would be required to switch the material to the on state making electronic programming effectively non-practical [Lac08b]. In fact, the maximum temperature rise T_{MAX} in the GST layer could be calculated as follows: $T_{MAX} = T_0 + V \cdot I \cdot R_{TH,eq}$, where T_0 is

the ambient temperature, and $R_{TH,eq}$ is the equivalent thermal resistance of the device. So, thanks to *Ovonic Threshold Switching*, the product $V \cdot I$ is sufficiently high even at relatively low V to have suitable T_{MAX} leading to crystallization of the amorphous matrix.

1.3.3 SET and RESET programming

Figure 1.3 shows the programming characteristic of a PCM cell [RaoWut], that is the dependence of the low-field cell resistance R as a function of the programming current. To obtain each curve, programming pulses of a given time duration and of increased amplitude are applied. After one programming pulse, the cell resistance R is read at 0.2 V. Before the next program pulse, the cell is brought again in the initial reference RESET state using a proper current pulse. Then, the measurement cycle starts again driving the cell with programming current pulses of a different time duration [Lac08b]. Three distinct regions can be recognized in the graph: (i) for programming pulses below 150 μA, the ON-state conduction (i.e. *Ovonic Threshold Switching*) is not activated and the very small current does not provide any phase change; (ii) in the 150–450 μA range, the resistance decreases due to the crystallization of the amorphous phase-change material, reaching the minimum resistance in the SET state; (iii) above 450 μA, the programming pulse melts some phase-change material close to the interface with the heater plug, leaving it in the amorphous phase. So, in this example, the PCM cell can be switched between the two SET and RESET states using current pulses of 400 μA and 600 μA, respectively. The pulses are independent of the initial cell state (resistance), thus cell can be therefore rewritten with no need of an intermediate erase [Lac08b] (this is, more precisely, the description of the "bit alterability" property introduced in Section 1.2.2). The minimum current which is able to bring the cell in the full RESET state (600 μA in Figure 1.3) is named RESET current, I_{RESET}. In the basic PCM cell like the one in Figure 1.1, the PCM and top electrode are planar layers deposited on a heater plug. The part of phase-change material effectively involved in the switching basically is a hemispherical volume on top of the heater. The relatively large I_{RESET} current, for the reasons that will be explained in Chapter 2, is one of the key factor that limits the performance of a PCM technology, both in terms of area and on energy consumption. To reduce the heating power (or program current), it is important to confine as much as possible the dissipated heat. While many different cell structures have been proposed in literature [RaoWut][Won10], optimization of the heat confinement is actually based on two simple principles: (i) by concentrating of the volume where effective Joule

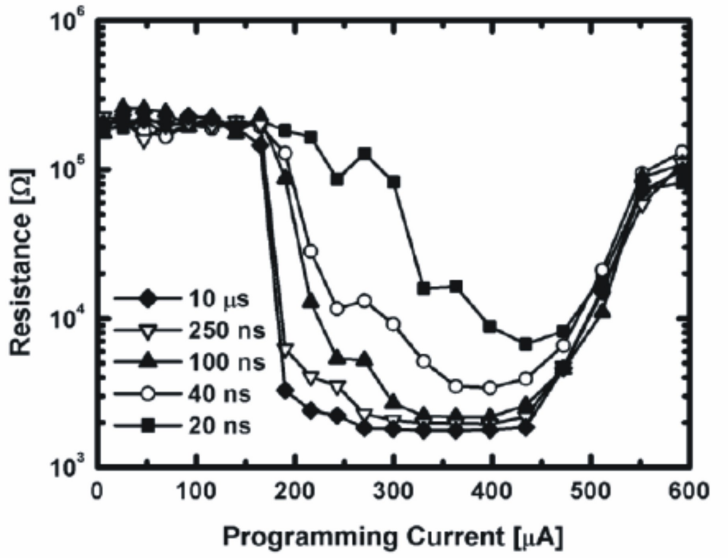


Figure 1.3: PCM programming characteristics, i.e. resistance as a function of the programming current for different programming pulse durations [RaoWut][Ott04].

heating takes place, and/or (ii) by improving the thermal resistance to reduce the heat loss to the surroundings [Lac08b]. Another way to reduce I_{RESET} is finding out new phase-change materials having i) lower melting temperature and/or ii) higher thermal resistivities.

1.3.4 Reliability

As for any other non-volatile memory technology, reliability is one of the major concerns. The main specific reliability issues of PCM are (i) data retention of the RESET state, affected by the (limited) stability of the amorphous state, (ii) endurance, limited by the occurrence of stuck at RESET or stuck at SET defects, and (iii) program and read disturbs, i.e. stability of the amorphous phase due to repeated thermal cycling caused by reading or programming neighboring cells. Examples of electrical experiments analyzing data retention and cycling characteristics of a PCM cells/technology are provided in Figure 1.6 and Figure 1.7, respectively.

1.4 Phase-Change Memory cells based on $Ge_{53}Te_{47}$

In this Section, we present an electrical characterization study on PCM cells fabricated at CEA-Leti integrating the phase-change GeTe material. These findings, published in the paper [Per10], provide an introductory framework for Chapter 2, where experimental

results on a novel GeTe-based material, i.e. Carbon-doped GeTe, will be presented. For consumer applications, data retention performance has to be guaranteed for ten years at 85°C, and GST complies with this request. On the other hand, still, open questions remain on how to ensure better data-retention performances and even address, with PCM, the embedded memory market. In order to fulfill the request of 125°C fail temperature after ten years, alternative phase-change (PC) materials are required. In the literature, a huge number of different PC materials have been investigated, [Mat05][Mor07]. In [Fan09], it has been shown that the GeTe material, on full-sheet deposition, presents higher crystallization temperature (i.e., 185°C) than GST (i.e., 145°C). In [Rao09], tests on a static tester on full-sheet GeTe evidenced a very fast crystallizing process, showing a minimum 30-ns time for the stoichiometric composition. In [Bru09], tests on devices confirmed this very fast SET operation, down to 1-ns stress time. However, all papers lack information on reliability. In this Section, we present a study on the electrical behavior of PCM based on a GeTe active material [Per10]. We compare electrical performances of PCM cells based on GeTe and GST, with the same pillar cell architecture. In particular, SET and RESET operations, endurance, and data retention are assessed. GeTe PCM show, first, extremely rapid SET operation (yielding a gain of more than one decade in energy per bit with respect to standard GST PCM), second, robust cycling, up to 10^5, with 30 ns SET and RESET stress time, and third, a better retention behavior at high temperature with respect to GST PCM. These results, obtained on single cells, suggest GeTe as a promising alternative material to standard GST to improve PCM performance and reliability.

1.4.1 Experimental results and discussion

Amorphous phase stability in blanket films

In order to evaluate the stability of the amorphous phase, 100-nm-thick co-sputtered amorphous GST and stoichiometric GeTe (53 : 47 ratio by RBS measurements) thin films were deposited on Si/SiO_2 substrates. Note that the PC materials have been deposited with a dc magnetron sputtering tool from monotargets of GST and GeTe, respectively. These films have been processed under argon atmosphere with a pressure of 0.005 mbar and a cathode power of 100 W at room temperature. The deposition rates for GST and GeTe are 6 and 6.2 /s, respectively. The resistivity of our samples were measured under isothermal conditions for different bake temperatures, see Figure 1.4(a) and (b) for GST and GeTe, respectively. It appears that GeTe retains the amorphous state at higher temperature compared with GST. By extrapolation from these

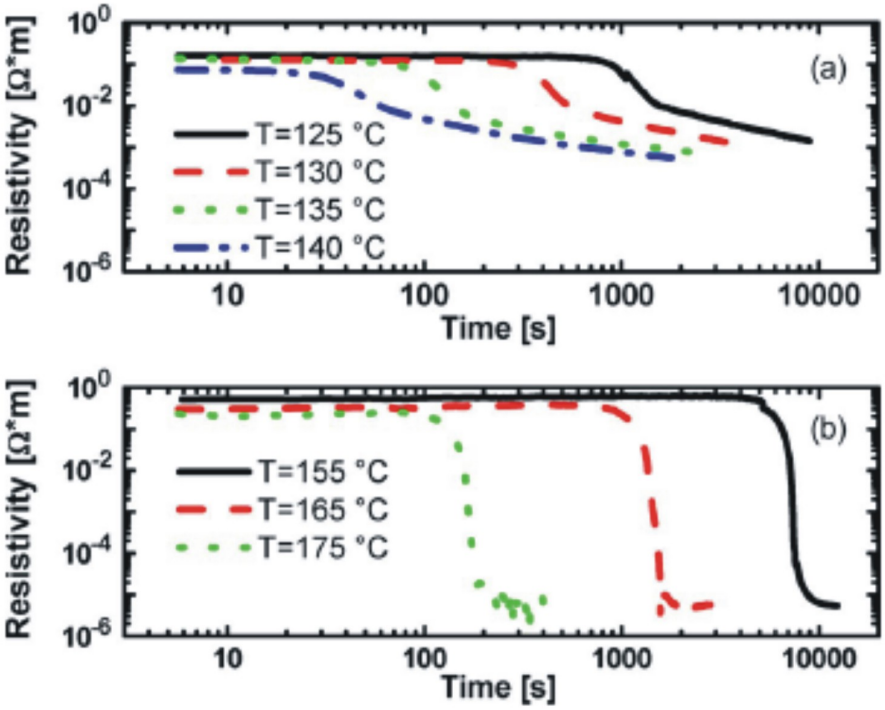


Figure 1.4: Resistivity measurements on blanket films of (a) GST and (b) GeTe. Measurements are made with a four-probe equipment and a Keithley 4200 parametric analyzer. In the same timescale, different temperatures are screened for GST and GeTe. GeTe confirms superior amorphous phase stability [Per10].

measurements, based on the Arrhenius law, it follows that GST provides a maximum 10 years fail temperature of around 75°C, with an activation energy of E_A = 3.13 eV, while the maximum fail temperature of GeTe is around 105°C, with E_A = 3.2 eV. These results represent an upper bound of the intrinsic retention properties of PC materials when integrated in actual devices [Coo95]-[Coo96]. Indeed, as-deposited materials are perfectly amorphous, while the melt-quenched amorphous material in PCM can have crystalline seeds (formed during the quench process) and is surrounded by the crystalline matrix: the crystallization process in actual devices can be facilitated. Note in Figure 1.4 the different shapes of isothermal measurements: in GeTe, as soon as a crystalline nucleus is formed, crystal growth is almost instantaneous and allows a contrast amorphous/crystalline resistivity of more than four decades; in GST, the crystallization process is much slower, featuring not more than two decades of resistivity drop at the transition from the amorphous phase.

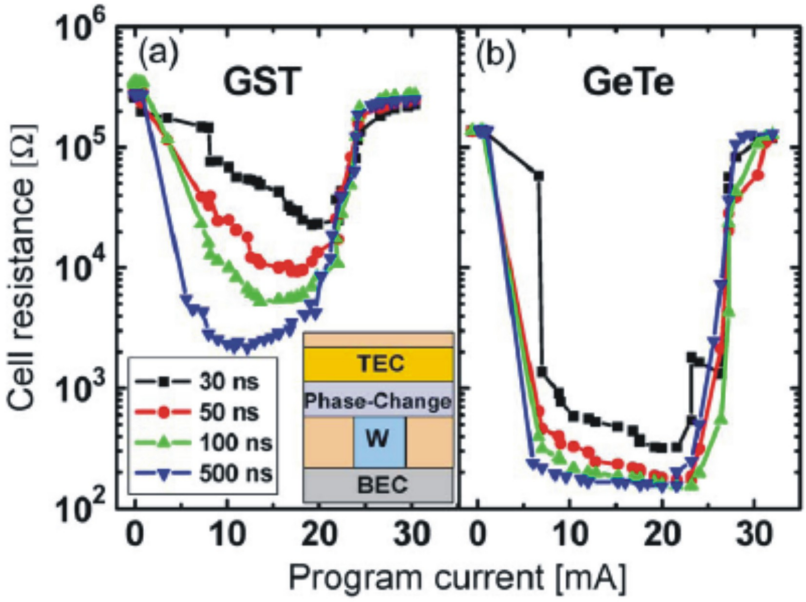


Figure 1.5: Programming performance for (a) GST and (b) GeTe devices with different SET times; each SET pulse is preceded by a fixed RESET pulse (I_{RESET} = 30 mA, t_{RESET} = 30 ns). Programming currents are high (due to large W plug). Values should be considered as terms of comparison between GST and GeTe. Note that GeTe shows much faster SET operation with a higher contrast between RESET and SET states than that of GST. (Inset) Schematics of the fabricated devices [Per10].

PCM Single Cells Performance and Reliability

GeTe and GST have been integrated in a simple pillar device architecture (see inset of Figure 1.5) with a 300-nm-wide W pillar in direct contact with a 100-nm-thick PC layer. A 20 nm in situ-deposited TiN layer and the upper top electrode finally complete the cell stack. A 200°C thermal annealing in nitrogen environment is performed at fab out to establish the device in the SET state, before starting the electrical characterization.

1) *Program Characteristics*:
The program characteristics of the integrated test structures were measured using a dedicated pulsed setup as described in [Fan09]. By using a pulse generator and an active probe, it was possible to read, by using a 100 Ω load resistor, the cell current for pulses down to 30 ns (2-ns rise/fall times). The relative programming speed of GST- and GeTe-based devices is shown in Figure 1.5. The SET pulse length was increased from a minimum of 30 ns to a maximum of 500 ns. It is apparent that while, in the case of GeTe, we have a good crystallization for all pulse lengths (with a minimum

resistance contrast of two orders of magnitude), in the case of GST, the final resistive value is much more sensitive to pulse length and amplitude. In other words, assuming a RESET/SET contrast criterion of two decades, the SET state in the GeTe device is achieved in 30 ns, while the SET state in the GST device is obtained in 500 ns: GeTe allows a gain of more than one decade in energy per bit with respect to GST. In agreement with amorphous/crystalline contrast on full-sheet depositions, note that the maximum achievable contrast is approximately three orders of magnitude for GeTe and approximately two for GST, with the crystalline state being much more conductive for GeTe. Moreover, the fast resistivity drop noticed for GeTe could justify the very fast transition between RESET and SET states (see Figure 1.5(b)).

2) *Endurance Characteristics*:
The results of the endurance test, with different SET times, are shown in Figure 1.6. In agreement with the results shown in Figure 1.5, for a 200 ns pulse, GST maintains a resistive contrast of about two decades between RESET and SET states (Figure 1.6(a)) while GeTe shows more than three decades (Figure 1.6(b)). In both cases, no cell failure is apparent up to 10^6 cycles. In the case of a short SET pulse, it is apparent that GST displays a narrower resistance window which closes as the cycle count increases Figure 1.6(c). On the contrary, GeTe shows a very good endurance up to 10^5 cycles with SET/RESET pulses as short as 30 ns (see Figure 1.6(d)).

3) *Data Retention Characteristics*:
In Figure 1.7, we have represented the data-retention characteristics for GeTe and GST. In these experiments, the chuck is heated up to high temperature, and then, the sequence (RESET pulse, plus repeated resistance measurements) is performed on 9 cells. As shown in the inset, similar average retention behaviors (i.e., resistance loss in the same timescale) are obtained at 160°C for GeTe and at 125°C for GST. These results suggest that amorphous GeTe has a better thermal stability than GST, in agreement with the higher crystallization temperature measured on full-sheet films (T_C around 185°C and 145°C, respectively [Fan09],[Rao09]).
A more uniform behavior in GST than that in GeTe devices seems to appear and should be better investigated. At the onset of the crystallization process, the crystallization speed is much higher in GeTe than in GST. The same effect has been noticed for blanket layers (Figure 1.4). This behavior can be related to the different interplays between nucleation and growth in the crystallization process, which is less known for GeTe [Rao09],[Coo95]-[Coo96]. Moreover, the stronger contrast, between crystalline

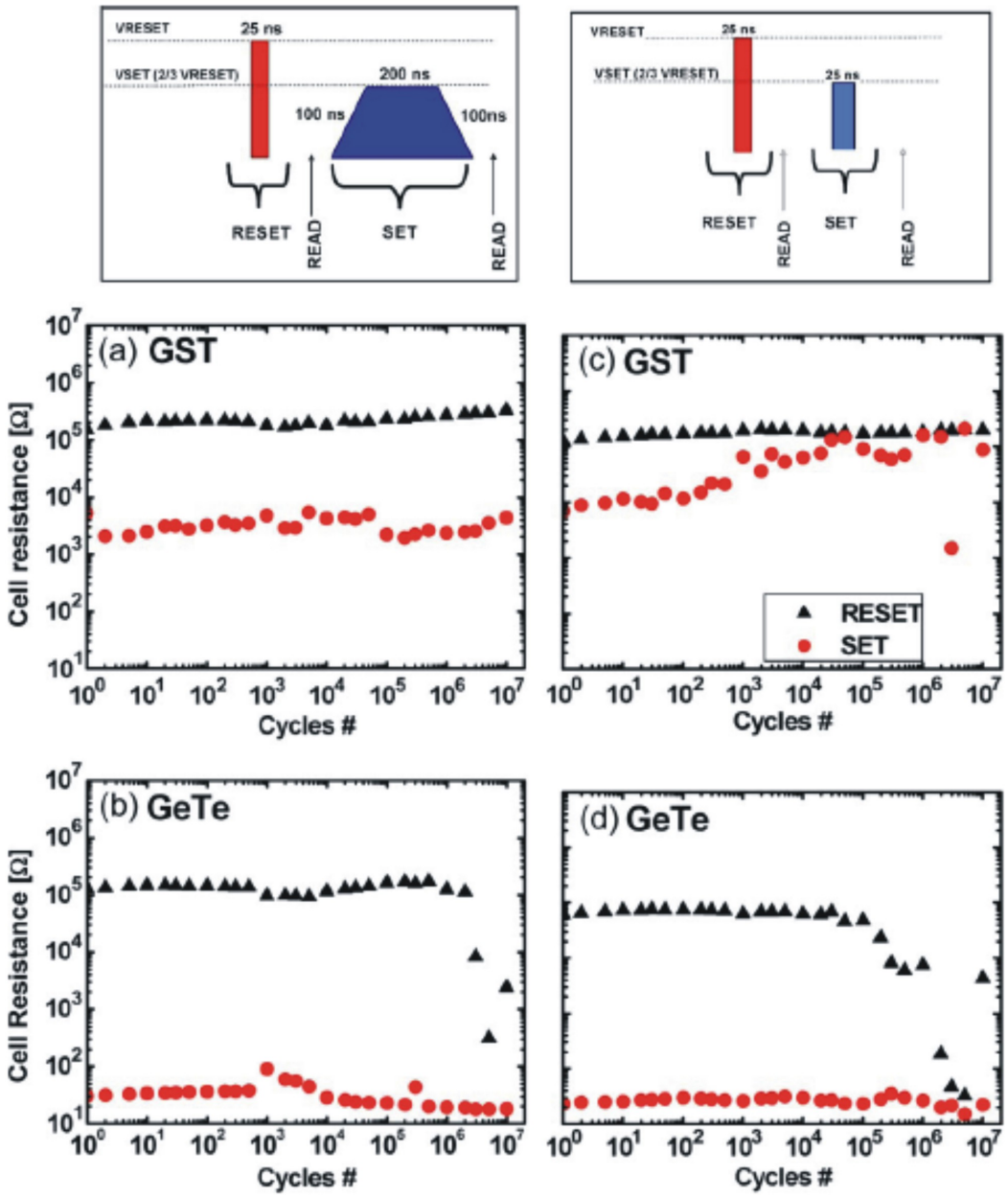


Figure 1.6: Endurance characteristics for (a)–(c) GST and (b)–(d) GeTe. In (a)–(b), a SET pulse of 200 ns is used to program the cells. In (c)–(d), a SET pulse of 30 ns is used. Note that no intelligent algorithm (i.e., variable number of pulses to maintain a fixed RESET/SET contrast) is used to cycle the cells and that I_{RESET} = 26 mA and I_{SET} = 18 mA for both GST and GeTe [Per10].

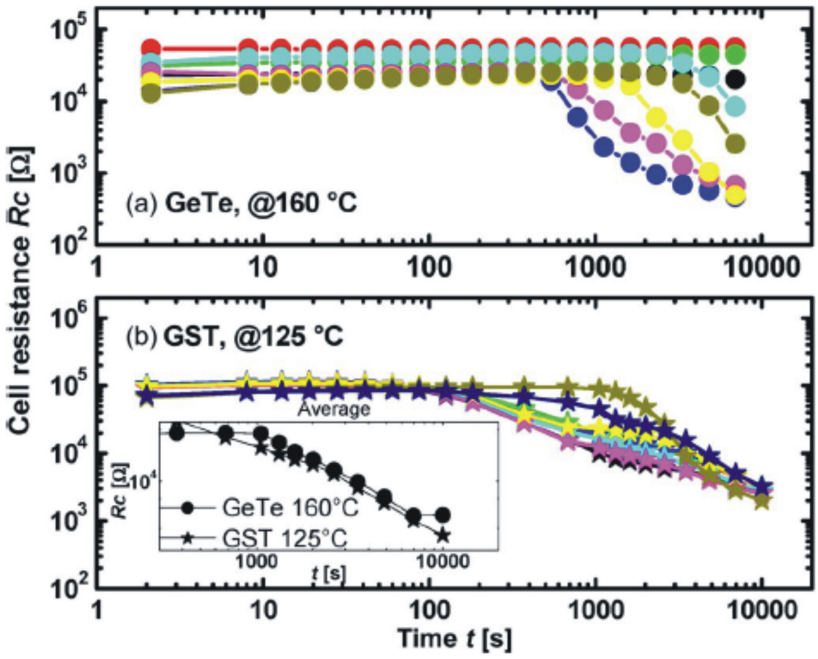


Figure 1.7: Data retention for 9 devices at (a) 160 °C for GeTe and (b) 125 °C for GST after identical RESET pulses I_{RESET} = 30 mA/ t_{RESET} = 60 ns. In the inset, the geometric average of the resistance evolution of GeTe and GST is the same during crystallization. Note that the reported retention experiments are performed for the same ratio T/T_M, where T_M is the material melting temperature equal to 903 and 996 K for GST and GeTe, respectively [Per10].

and amorphous resistivities, in GeTe than that in GST (see Figure 1.5) could justify a faster drop in cell resistance as soon as a crystalline path is created through the amorphous spot.

1.4.2 Conclusions

To conclude, we argue that:

- GeTe devices show very fast program characteristics (in agreement with the literature [Bru09]), allowing a gain of more than one decade in energy per bit with respect to GST, for SET operations. The RESET/SET contrast is approximately three decades for GeTe, while it is approximately two decades for GST, with the SET state being more conductive in GeTe than in GST.

- GeTe devices allow stable endurance up to 10^5 cycles with RESET/SET pulses as short as 30 ns.

- Similar data-retention characteristics are shown for GeTe at 160°C and for GST at 125°C. This result agrees with the difference in crystallization temperatures measured on full-sheet films and noticed in [Fan09] and [Rao09].

These data shed new light on GeTe as an alternative material to GST in PCM, eventually allowing us to address applications where programming speed and bandwidth are requested (i.e., caching) or where strict requirements on data retention at high temperatures exist (i.e., embedded NVM).

Chapter 2

Carbon-doped GeTe: a promising material for Phase-Change Memory

2.1 Abstract

This chapter investigates Carbon-doped GeTe (GeTeC) as novel material for Phase-Change Memories (PCM). In the first part of the manuscript, a study of GeTeC blanket layers is presented. Focus is on GeTeC amorphous phase stability, which has been studied by means of optical reflectivity and electrical resistivity measurements, and on GeTeC structure and composition, analyzed by XRD and Raman spectroscopy. Then, electrical characterization of GeTeC-based PCM devices is reported: resistance drift, data retention performances, RESET current and power, and SET time have been investigated. Very good data retention properties and reduction of RESET current make GeTeC suitable for both embedded and stand-alone PCM applications, thus suggesting GeTeC as promising candidate to address some of the major issues of today's PCM technology.

2.2 Introduction

Phase-Change Memory (PCM) is widely recognized as one of the most promising next-generation non-volatile memory technologies and a present valuable alternative to the Flash mainstream [Bez09].

PCM is based on the reversible electrothermal-induced phase transition of a chalcogenide alloy between an amorphous high-resistance state (named RESET) and a polycrystalline low-resistance one (SET). So far, the most known and used chalcogenide

material for PCM applications is an alloy made by Germanium, Antimony and Tellurium: $Ge_2Sb_2Te_5$ (GST). To program the memory cell, suitable pulses inducing Joule heating inside the chalcogenide material are needed to switch the device between the two phases. The transition from polycrystalline to amorphous material is referred to as the RESET operation, while the crystallization of the amorphous chalcogenide matrix is named SET. The RESET operation is accomplished by delivering to the memory cell a relatively high current pulse (in the order of few hundreds of microamperes for the current more scaled technologies), followed by fast quenching. The current pulse brings the chalcogenide material up to the melting point and then stucks it into an amorphous phase. Lower but longer current pulses (in the range of hundreds of nanoseconds) are used to appropriately heat the active material and arrange it in the ordered polycrystalline form. Concerning PCM data retention, while the polycrystalline phase of the chalcogenide material is inherently stable, being the lowest possible energetic state of the system, retention instability affects the amorphous phase through two physical phenomena: spontaneous crystallization and low-field conductivity drift[Iel07].
Unlike Flash, PCM offers low-voltage operation and direct write. Moreover, at cell level, PCM has potential of better scalability (down to few nanometers [Rao08]), highest endurance (up to 10^9 programming cycles [Ser09]), and faster programming speed (in the order of few nanoseconds [Bru09]). Furthermore, GST can guarantee stability of programmed amorphous bits for more than 10 years at 85°C [Gle07]. Nevertheless, to provide high-performance and reliable devices suitable for a broad range of memory applications and thus compete with current non-volatile memory technologies, two main issues have to be addressed: the reduction of the current needed to RESET the device in order to increase the memory density, and the improvement of the stability of the amorphous state to boost PCM data retention performances.
Focusing in particular on RESET programming, two main issues impact the intrinsic performances of the PCM device when integrated in a memory array. First of all, since the RESET current is high, large series selectors are needed, thus limiting the exploitation of PCM intrinsic scaling capability. This phenomenon makes today's GST-based PCM to be not competitive with Flash NAND in terms of density, and so cost [Lam08]. Secondly, the high RESET current makes relatively low the programming bandwidth, reducing the number of cells that can be programmed at the same time. In fact, while the programming time of the PCM device is about three orders of magnitude lower compared to that of Flash memory cells, almost all the advantage is lost at the array level, where PCM and Flash both feature programming bandwidth in the order of about 10 Megabits per second [Bez09].

For these reasons, a reduction of the RESET current would greatly boost PCM performances, encouraging PCM employment in particular for stand-alone applications. Furthermore, even if GST data retention is sufficient for consumer applications, many efforts are today devoted to improve the high temperature reliability of PCM technologies in order to address also the embedded memory market.
In this framework, we propose an experimental study of C-doped GeTe chalcogenide alloy (GeTeC) as possible solution to the previous mentioned issues [Bet10a][Bet10b]. GeTeC is based on the Germanium Telluride alloy, named GeTe. GeTe is a good alternative to the reference PCM material GST. In particular, GeTe provides faster SET, GST-like endurance, and better data retention compared to GST [Bru09][Fan09][Per10]. Moreover, there are basically three reasons that explain why doped-GeTe is worth investigating, and why carbon could be a preferential dopant candidate. The first reason is that there are many examples of RESET current reduction when dielectric impurities are introduced in a phase-change host, like nitrogen-doped GST [Hor03], oxygen-doped GST [Mat05], GST doped with SiO_x, SiN_x, SiC_x and carbon [Czu06]. This effect could be due to the fact that low-conductive inclusions replace part of the programming volume and minimize the heat loss in the phase-change layer [Mat05][Czu06], and/or since the doping impurities increase the dynamic electrical resistivity of the chalcogenide material [Ahn04]. Secondly, doping could also improve data retention performances, both in terms of increase of 10 years fail temperature than of activation energy, as shown in [Mor07] for doped InGeTe, and in [Czu10] for SiO_2-doped $Ge_4Sb_1Te_5$. The beneficial effect of doping for data retention could be justified by the fact that the dopants, arranged in a disordered configuration inside the phase-change material, could pile up at the grain boundaries, keeping the crystalline grains from growing large [Kim07]. Finally, to understand why carbon could be an interesting dopant material, consider that CVD tools are supposed to become more and more important to fabricate PCM devices for the future technology nodes, and carbon can be easily introduced with CVD using organometallic precursors (e.g. $Ge[N(CH_3)_2]_4$ and TeC_6H_{14}) or specific gas (e.g. CH_4).
The Chapter is organized as follows. In section 2.3 we investigate the properties of GeTeC blanket layers focusing specially on amorphous phase stability investigated by optical reflectivity and electrical resistivity measurements. Moreover, physico-chemical characterization, i.e. X-ray Diffraction (XRD) and Raman spectroscopy, is described. Section 2.4 is dedicated to electrical characterization of simple GeTeC-based PCM test cells. We report experimental data on cell data retention, analyzing failtime variability and 10 years fail temperature extrapolation. Besides, experimental data on RESET current and RESET power are presented. Finally, we show R-V programming charac-

teristics, fixing our attention on SET programming time. In the paper, two different carbon doping percentages are analyzed: GeTe with 4% C and GeTe with 10% C (named GeTeC4% and GeTeC10%, respectively). Comparative data on GeTe and on the reference PCM material GST are also provided.

2.3 Material characterization: GeTeC blanket layers

100 nm-thick amorphous GeTe and GeTeC blanket layers were fabricated by plasma-assisted co-sputtering using two targets (stoichiometric GeTe and C) in Ar atmosphere at a pressure of 0.005 mbar and at room temperature. In order to screen the effect of carbon doping in the GeTe alloy, two different carbon impurity fractions were obtained by varying the polarization of the targets. Their percentages, revealed by Rutherford Back-Scattering (RBS) and Nuclear Reaction Analysis (NRA) measurements, are: GeTe with 4% carbon and GeTe with 10% carbon (named GeTeC4% and GeTeC10%, respectively).

2.3.1 Amorphous phase stability

Amorphous phase stability on blanket GeTe and GeTeC layers have been studied by optical characterization (i.e. optical reflectivity monitoring as a function of temperature) and by electrical characterization (i.e. electrical resistivity monitoring as a function of temperature).

Optical reflectivity

Figure 2.1 shows the optical characterization (i.e. optical reflectivity as a function of temperature T) carried out on our samples. We note that 4% carbon doping improves the amorphous phase stability compared to GeTe. In fact, GeTeC4% features a crystallization temperature (i.e. the temperature corresponding to an increase of 5% of the amorphous state reflectivity value) $T_C \sim 290$°C, while for GeTe $T_C \sim 180$°C. Further raising the carbon content yields a slower increase of the crystallization temperature (GeTeC10% $T_C \sim 340$°C, one of the highest ever reported in literature). Note that the transition between low-reflectivity amorphous state and high-reflectivity crystalline state, abrupt for GeTe, becomes smoother when C is added.
Then, optical reflectivity measurements at different baking temperatures have been performed to monitor the amorphous-to-crystal transitions and extract associated fail times $\tau_{F,opt}$ (i.e. the times at which the reflectivity increase of 5% with respect to the

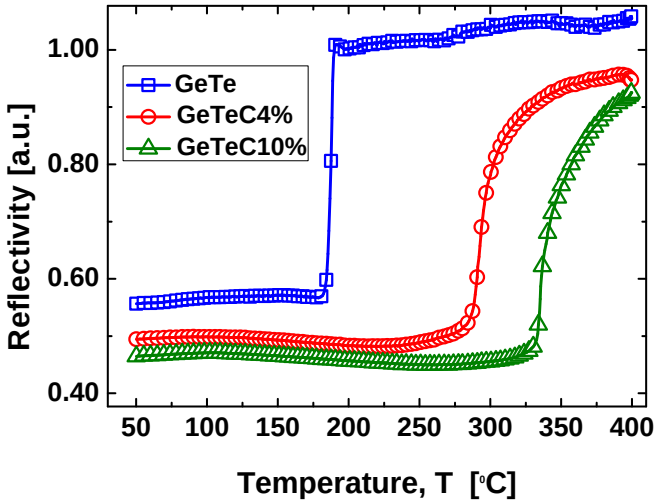


Figure 2.1: Optical reflectivity as a function of temperature for GeTe, GeTeC4% and GeTeC10% blanket layers. Chuck temperature is ramped up with a constant rate of 10°C/min, while reflectivity is constantly monitored. The sudden transition is the signature of the crystallization process.

amorphous characteristic value). As displayed in Figure 2.2 the fail times follow a typical Arrhenius law. It is worth noting that the activation energies E_A of GeTeC4% and GeTeC10% are about a factor two higher than the GeTe one. This suggests that GeTeC could provide both good data retention (related to amorphous stability) and also good programming performances (related to crystallization velocity). In fact, a high activation energy is necessary to achieve $\tau_{F,opt}$ in the ns range when the device reaches the very high programming temperatures (thus offering fast programming performance), and $\tau_{F,opt}$ in the range of years at device standard operation temperatures (thus offering good data retention characteristics).

Electrical resistivity

The results of optical reflectivity are confirmed by the 4-probes resistivity measurements shown in Figure 2.3, where electrical resistivity is plotted as a function of temperature. Once again, the crystallization temperature T_C increases with C doping concentration. Furthermore, as pointed out previously on the reflectivity curves, the transition is much sharper for GeTe than for GeTeC, suggesting once more that carbon doping leads to a slower crystallization speed.

To conclude, both optical and electrical characterizations, performed on blanket chalcogenide films, clearly highlight a strong rising of the crystallization temperature and

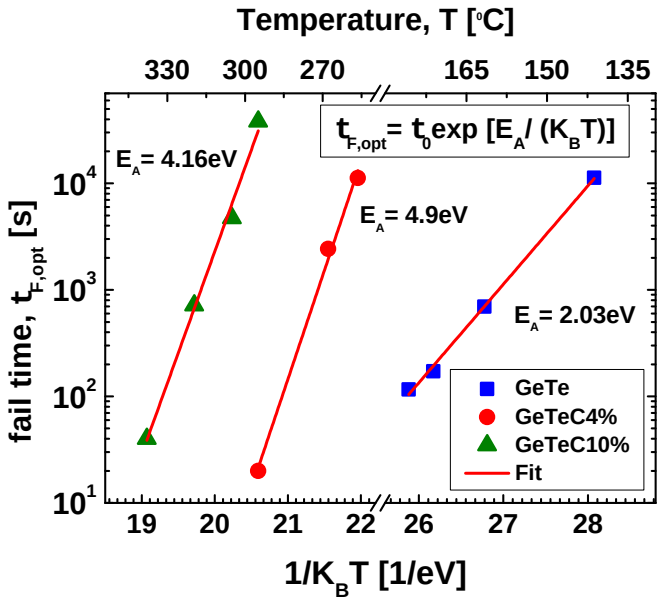


Figure 2.2: Retention fail time $\tau_{F,opt}$ as a function of $1/(K_B T)$ for GeTe, GeTeC4% and GeTeC10% blanket layers (symbols are data, line is fitting based on the Arrhenius law annotated in the figure). The E_A values extracted from the fitting of each curve are indicated in the graph.

of the associated activation energy with carbon doping, suggesting a potential improvement of data retention for PCM cells employing GeTeC instead of pure GeTe.

2.3.2 Structure and composition

Physico-chemical measurements have been performed to acquire an in-depth knowledge of both GeTeC structure and composition.

XRD measurements on crystalline films are displayed in Figure 2.4. XRD grazing angle measurements point out that GeTeC shows the same rhombohedral structure than GeTe. Figure 2.5 shows Raman spectra of GeTe and GeTeC thin films. Spectral responses of amorphous samples (see Figure 2.5(a)) present features around 80, 125, 175 and 250 cm^{-1}, which are characteristic of stoichiometric GeTe [And06]. The smoother shapes of the GeTeC Raman spectra with respect to the GeTe one suggest that adding carbon leads to an higher degree of disorder in the amorphous phase of the material, featuring a broader distribution of bond lengths and angles. Raman spectra of annealed GeTeC (see Figure 2.5(b)) show two-bands shapes assigned to crystallized materials [Kol04]. Then, with carbon content, the absence of the band around 300 cm^{-1}, which is characteristic

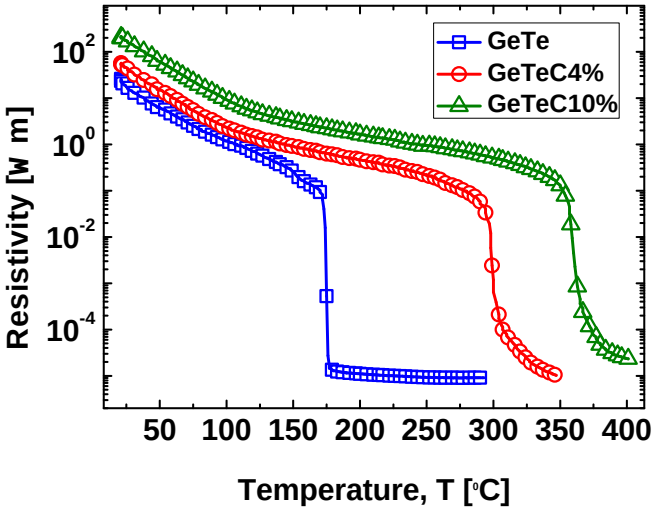


Figure 2.3: Electrical resistivity as a function of temperature for GeTe, GeTeC4% and GeTeC10% blanket layers. Chuck temperature is ramped up with constant rate of 10°C/min, while resistivity is constantly monitored. Sudden transition is the signature of the crystallization process.

of the precipitation of crystalline Ge embedded in a crystalline GeTe phase, may be an indirect proof of the formation of an amorphous Ge-C phase [Gou09]. Finally, the whole amorphous and crystalline shapes show few differences whatever the carbon doping, hence revealing quite similar microstructures.

To resume the main findings of the structural and compositional study here presented, we argue that the characterization of blanket samples reveals that the addition of carbon increases the disorder level of the amorphous phase of the material. Indeed, this is in agreement with the high crystallization temperature of GeTeC. In fact, the higher the disorder degree of GeTeC amorphous state, the higher the energy required to arrange it in an ordered rhombohedral crystalline form.

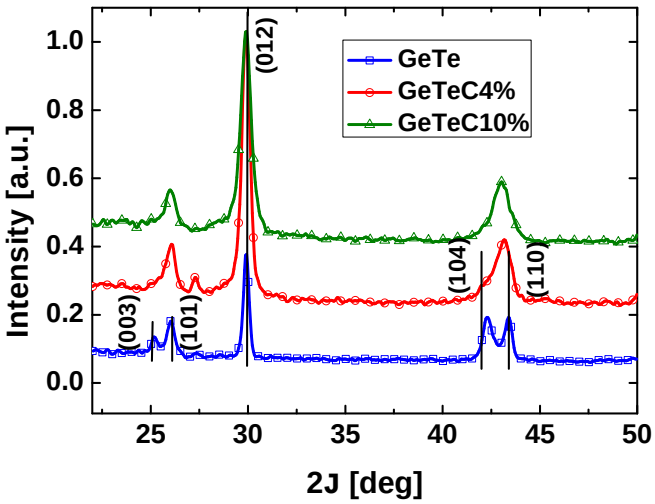


Figure 2.4: XRD grazing angle patterns of GeTe, GeTeC4% and GeTeC10%. Diffracted x-rays intensity is plotted against Bragg angle. The (003) and (101) reflections are characteristic of rhombohedral GeTe.

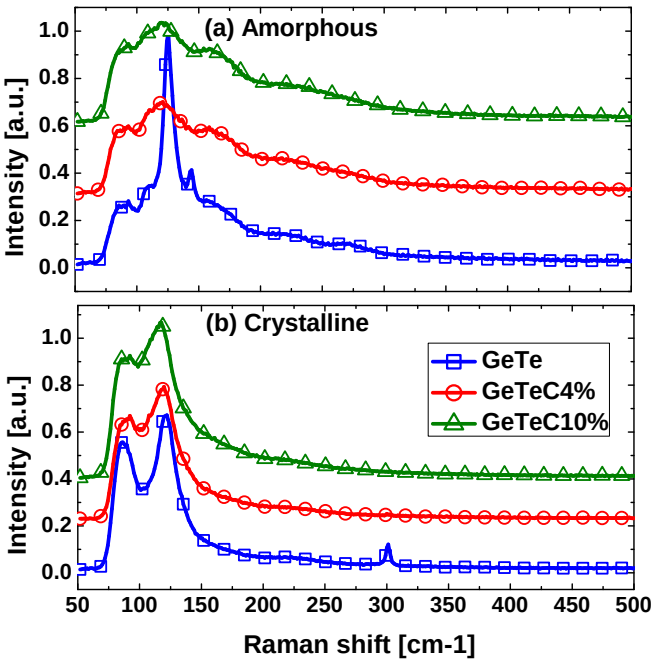


Figure 2.5: Raman spectra of amorphous (a) and crystalline (b) blanket layers of GeTe, GeTeC4% and GeTeC10%, respectively.

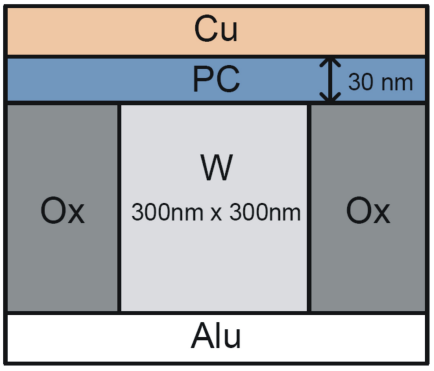


Figure 2.6: Schematic of the cross section of our lance-type PCM device (not to scale). The core of the memory cell is a 30 nm thick chalcogenide phase-change layer, indicated as PC in the figure, placed on a 300 nm wide and 300 nm thick tungsten plug, W, and insulating material, Ox. Top and bottom electrodes are Cu and Alu, respectively.

2.4 Device characterization: GeTeC-based PCM devices

To characterize the electrical behavior of GeTeC integrated in memory cells, simple lance-type PCM devices were fabricated. In our cells, a 300 nm wide and 300 nm thick W pillar is in direct contact with a 30 nm thick phase-change layer, see Figure 2.6. The GeTeC material has been deposited by plasma-assisted co-sputtering from 2 targets (stoichiometric GeTe and C) with same conditions in terms of atmosphere, pressure and temperature than of the blanket layers (see section 2.3).

2.4.1 RESET state stability

In order to explore the role of carbon with respect to time instability of amorphous phase in integrated PCM devices, we investigated Low-Field (LF) resistance drift and data retention (i.e. spontaneous crystallization) at high temperature. For both investigations, the PCM cell is programmed in the amorphous phase, and then the resistance is monitored as a function of time.

Resistance Drift

It has been shown that the resistance of amorphous PCM after RESET programming increase with time. The most accredited theory on PCM resistance drift explains this phenomenon as annealing of localized states in the the framework of a structural relaxation phenomenon. Since these localized states are the ones who enable the electronic conduction (hopping-like process), the reduction of the number of this traps

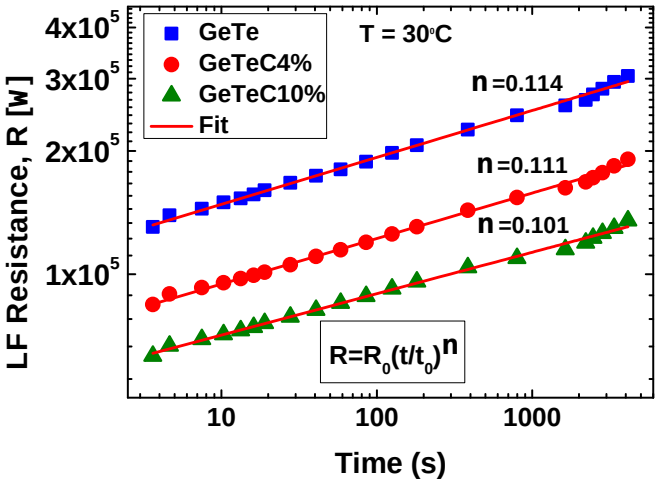


Figure 2.7: Low-Field (LF) resistance as function of time for PCM cells programmed in amorphous phase. Each point of the curves has been obtained by averaging results obtained on 9 different devices. During the experiment the temperature T is fixed constant at 30°C.

for a given volume due to traps annealing leads to an increase of the electrical resistance of the memory cell. [Iel07]. LF resistance drift and spontaneous crystallization play their major role at different time scales. In fact, at relatively short times after RESET programming, the drift effect, correlated with the increase of the cell resistance, becomes evident. However, at higher times, drift is overcome by spontaneous crystallization, leading, on the contrary, to the drop of the cell resistance value [Gle07]. As known, the time evolution of low-field resistance of amorphous cells obeys the empirical relation $R = R_0(t/t_0)^\nu$, where R_0 is the resistance cell observed at t_0 time instant, and the exponent ν gives the slope in the bilogarithmic plot of R as a function of time t [Iel07]. Resistance drift data of cells programmed in the RESET state are shown in Figure 2.7. We note that ν value slightly decreases with the carbon content, varying from 0.114 (GeTe) to 0.101 (GeTeC10%).
This small decrease of ν with C concentration suggests that the annealing mechanisms of traps in GeTeC is not much affected by carbon content. Therefore, C should play a negligible role for what concerns amorphous structural stability in the time scale in which low-field resistance drift is appreciated.

Data retention

In Figure 2.8 data retention measurements performed at 170°C on PCM cells with amorphous GeTe, GeTeC4% and GeTeC10% are shown. The initial drift is clearly

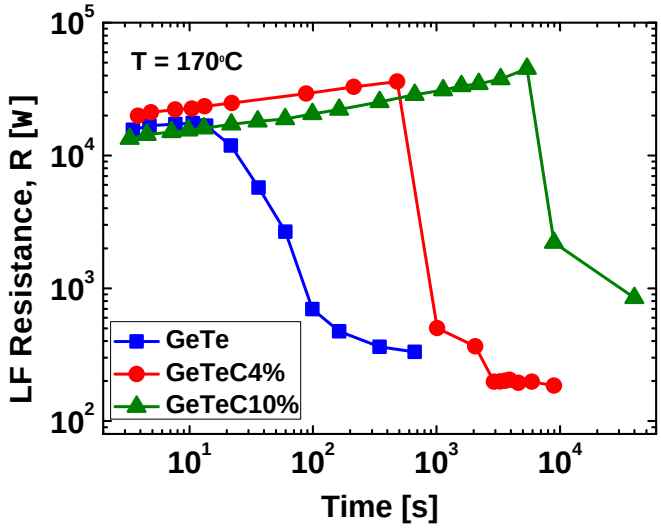


Figure 2.8: Data retention measurements on PCM cells integrating GeTe, GeTeC4% and GeTeC10% at a temperature of 170°C. Each cell has been programmed with the same amorphization pulse and then LF resistance has been monitored. Each curve is representative of tests performed on 30 cells, on average.

visible in all the characteristics. Then, the resistance falls down owing to spontaneous crystallization. Note that the resistance drop significantly shifts at higher times as the carbon concentration is increased. In particular, defining the electrical fail time $\tau_{F,ele}$ as the time corresponding to a decrease of 50% of the initial programmed RESET resistance value, it turns out that the GeTeC10% fail time is almost two orders of magnitudes longer with respect to the $\tau_{F,ele}$ of pure GeTe. In Figure 2.9 the GeTeC10% mean fail times are recorded for five different temperatures (155°C, 160°C, 170°C, 175°C, and 180°C) and then 10 years extrapolation is obtained simply applying Arrhenius law. The E_A extracted value, 4.33 eV, is in good agreement with optical characterization on blanket material depositions (i.e. 4.16 eV). It is worth noting that the 10 years fail temperature extrapolated for GeTeC10%-based PCM devices is about 127°C suggesting that GeTeC10% addresses the specifications of embedded memories.
Furthermore, in Figure 2.10 the dispersion of fail times of GeTeC10% and GeTe PCM is compared. The graph displays the ratio between fail time standard deviation (σ) and mean value (μ) for three different temperatures: 160°C, 170°C and 180°C. In each measurements the PCM cells are programmed in the amorphous state and then LF resistance is monitored. The results on about 20 cells show that carbon addition has a beneficial effect not only in rising the mean fail time, but also in reducing the fail time distribution. In fact, for each temperature, GeTeC10% has a reduced fail time dispersion, featuring a lower σ/μ. The evidence that fail time variability is reduced

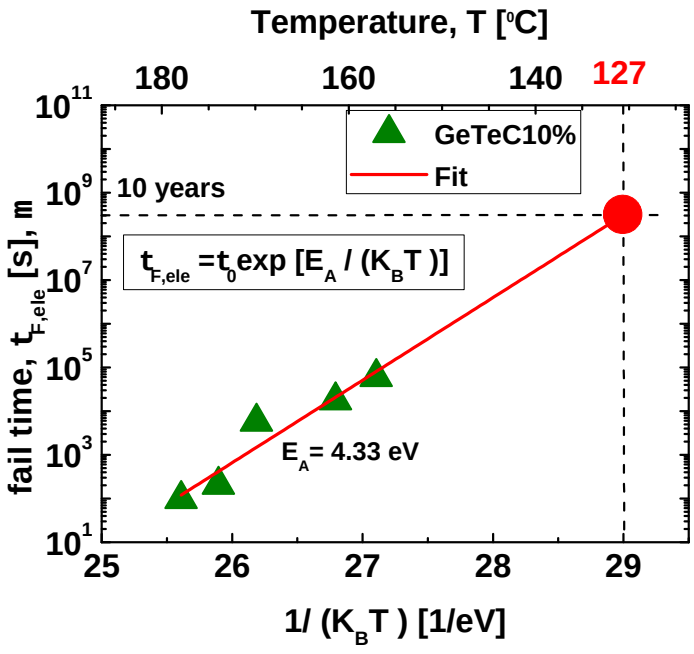


Figure 2.9: Electrical fail time mean value μ as a function of $1/(K_B T)$ for GeTeC10% PCM-based devices (K_B is the Boltzmann constant). Symbols are data, line is fitting based on the Arrhenius law annotated in the figure. The E_A value, extracted from the fitting, is indicated in the graph. Each point has been obtained averaging measurements on about 30 cells.

thanks to C doping suggests that GeTeC grain size is smaller compared to GeTe. In fact, it has been show in literature that, for a given volume, the higher the number of grains, the lower the dispersion of data retention performances [Rus07].
The data retention experiments on PCM devices clearly show that C doping improves GeTe stability to high temperature stress, increasing 10 years fail temperature extrapolated and activation energy, thus confirming the conclusion drawn by the previous material characterizations. Furthermore, C doping also decreases the fail time statistical distribution, probably by means of lowering the grain size of the crystalline matrix.

2.4.2 Programming Characteristics

RESET programming has been investigated by means of R-I characterization, fixing the attention on RESET current and power. R-V measurements are used to analyze the SET operation with focus on SET time.
Note that, due to the fact that our fabrication process features 200°C maximum temper-

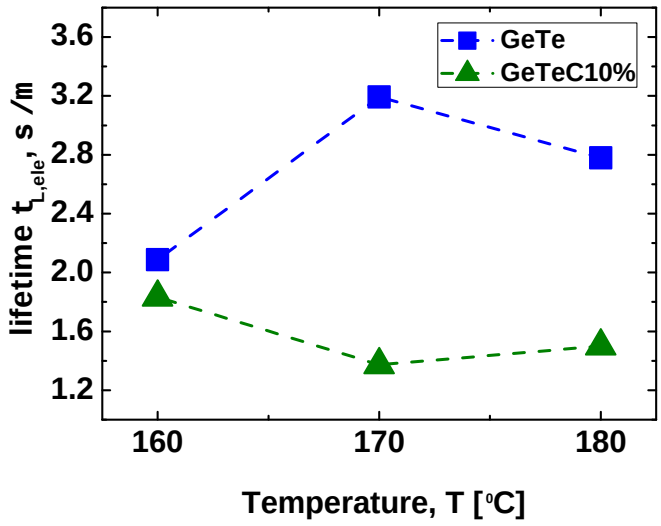


Figure 2.10: Electrical fail time standard deviation (σ) / mean value (μ) for GeTe and GeTeC10%-based PCM devices for three different temperatures. Each point has been obtained averaging measurements on about 30 cells.

ature, the devices exhibited an as-deposited amorphous state at fab-out. Our characterization therefore was initiated by an "electrical" anneal whose intent was to crystallize at maximum our devices. For that we typically used μs-long and 5V-high pulses.

RESET Current and Power

Figure 2.11 shows data of RESET programming for GST, GeTe, GeTeC4% and GeTeC10%-based PCM. The electrical setup employed for these measurements is described in [Fan09]. The PCM cell is programmed with 50 ns width pulses of increasing current amplitudes and very fast 10 ns trailing edge (I_{PROG} pulses). After each pulse the LF resistance is measured. Each programming pulse is preceded by a SET pulse, in order to analyze the effect of the increasing amplitude of programming signals starting from the same polycrystalline SET state. We define the current to RESET the device, I_{RESET}, as the I_{PROG} needed to obtain the 90% of the maximum LF resistance value of the whole SET-to-RESET transition. Note that the minimum SET resistance values of the curves stay within technological variability, while SET resistance mean values are shown in Figure 2.14. The mean values of I_{RESET} are plotted for each material in Figure 2.12. Interestingly, I_{RESET} lowers as the carbon percentage rises. In fact, while in first approximation GST and GeTe are characterized by a comparable RESET current (I_{RESET} GeTe $\sim 95\%$ I_{RESET} GST), a reduction of more than 10% is obtained for GeTeC4%, and of more than 30% for GeTeC10%. Note also that the

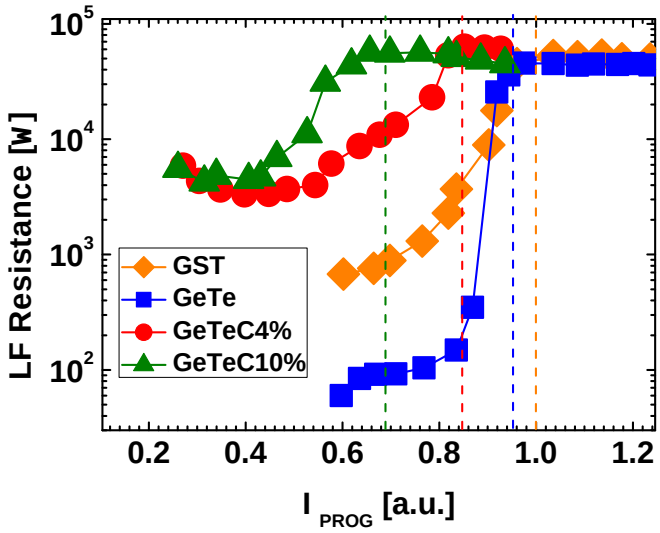


Figure 2.11: SET-to-RESET transition for GST, GeTe, GeTeC4% and GeTeC10% PCM. LF device resistance is plotted against programming current I_{PROG}, in normalized unit (I_{RESET} of GST is set to 1). Before each I_{PROG} pulse a SET pulse is applied to the cell in order to re-initialize the PCM to the same SET state. Vertical dash-type lines trace the correspondence $I_{PROG} = I_{RESET}$ for each alloy. The curves are representative of about 10 devices.

RESET resistances are similar for each material, suggesting that the resistivity of the four different alloys in the amorphous melt-quenched state should be practically the same. It is worth noticing that in previous works focusing on other systems always made by a chalcogenide alloy with dielectric co-sputtering inclusions, i.e. C-doped GST and GST with SiO_x or SiN_x dopants, the RESET current diminution has been interpreted as a consequence of the effective reduction of the thermal conductivity of the phase-change material [Czu06][Lee09]. In particular, the decrease of the *effective* thermal conductivity of the active layer has been correlated with the *actual* reduction of the chalcogenide programmable volume caused by the formation of nanoclusters of immiscible chalcogenide-dielectric mixtures. Interestingly, the electrical properties of C-doped GST, GST-SiO_x and GST-SiN_x systems have many analogies with the ones of GeTeC, namely: a) better data retention, i.e. significant increase of 10 years fail temperature and activation energy[Czu10] b) important reduction of the RESET current with doping, c) increase of the SET state cell resistance of the doped material compared to the undoped one (see Figure 2.14) and d) resistivity of the melt-quenched amorphous phase doping independent [Czu06].
Furthermore, using the I_{RESET} value previously obtained, it is possible to calculate the

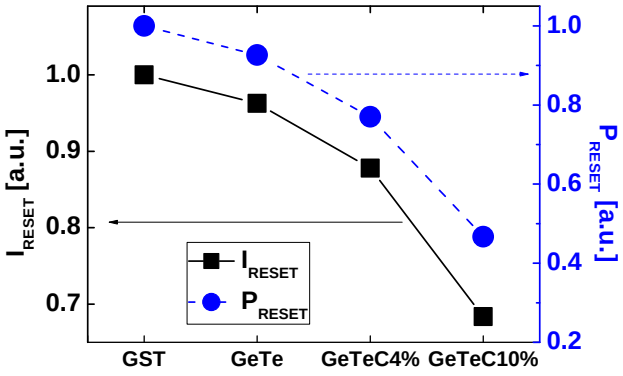


Figure 2.12: Mean values of RESET current (left) and RESET power (right) for GST, GeTe, GeTeC4% and GeTeC10%. Data are normalized compared to the GST ones. Each point is obtained averaging on 10 PCM devices.

power associated with the RESET operation P_{RESET} as $P_{RESET} = I_{RESET} \cdot V_{RESET}$, where V_{RESET} is the voltage of the RESET pulse, which characterization is shown in Figure 2.13. The V_{RESET} required to RESET the device decreases when C is increased. In fact, to achieve a high resistance value, a 9V pulse is needed for GST and GeTe-based cells, while in GeTeC4% case the RESET voltage is lower (around 8V), and for GeTeC10% even a 6V pulse is sufficient. This leads to a P_{RESET} reduction of more than 20% for GeTeC4% and of more than 50% for GeTeC10%. Figure 2.12 compares RESET current and power normalized values for the materials under investigation. It is worth noticing that the RESET power reduction in GeTeC is not directly linked to an increase of the electrical resistivity of the chalcogenide in the liquid phase, like what claimed for N-doped GST [Ahn04]. In fact, being the conductivity of the melt chalcogenide material very high, the resistance of our PCM test devices in the programming region results dominated by the metal lines and the plug [Bet10b]. For this reason, slight variations of the resistivity of the chalcogenide material in the programming region, *if any*, are very difficult to quantify.
To resume, the analysis of the RESET curves clearly highlights that C doping significantly reduces both RESET current and RESET power.

SET Time

Program characteristics (i.e. R-V tests, see Figure 2.13) have been measured using the experimental setup for pulsed measurements described in [Tof10]. For each material, several R-V measurements have been performed, varying the SET pulse width from

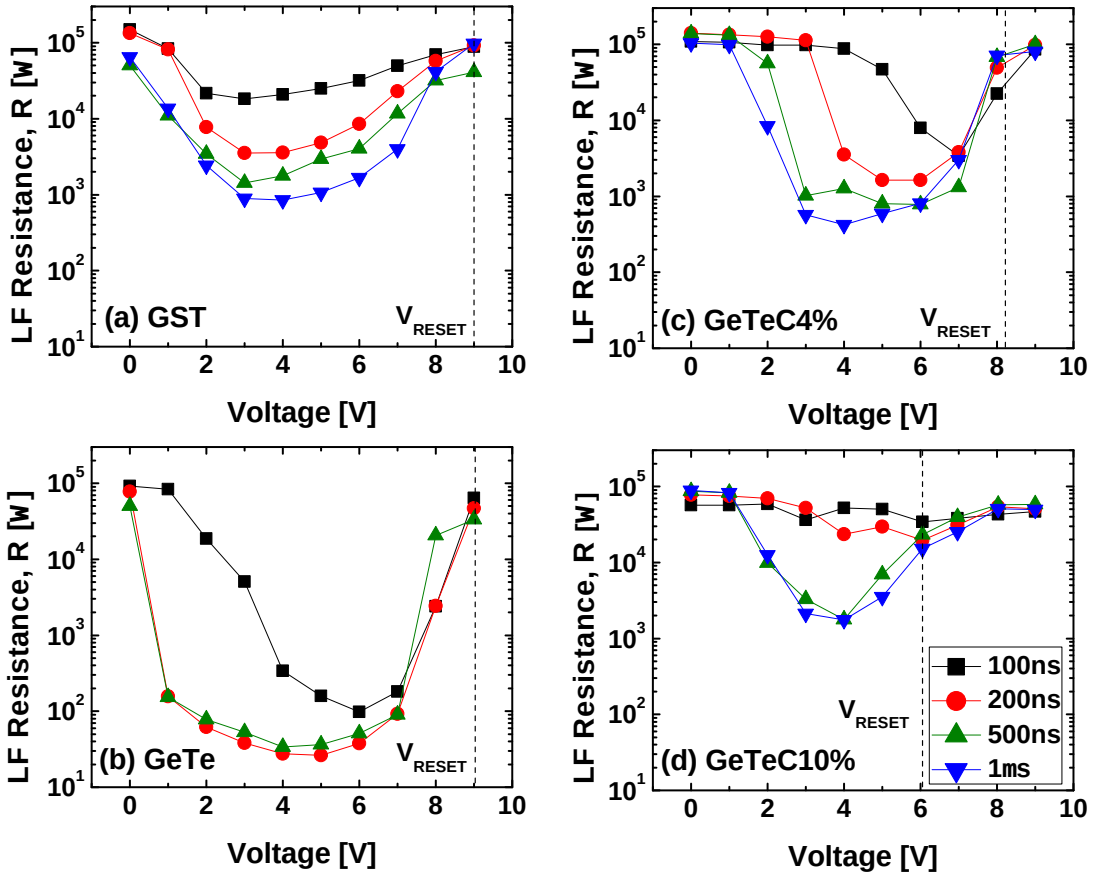


Figure 2.13: R-V characterization on PCM cells with (a) GST (b) GeTe, (c) GeTeC4% and (d) GeTeC10% materials. Different SET time pulse widths (100 ns, 200 ns, 500 ns, and 1 μs) have been applied to the cells and then LF resistance is read. Each SET pulse is preceded by a fixed RESET pulse (amplitude= 9V, width= 100ns, fall= 10ns). The voltage values V_{RESET} needed to obtain the RESET state are indicated by dash-type vertical lines for each R-V characteristics.

a minimum of 100 ns to a maximum of 1 μs. We observe that GeTeC appears slower than GeTe. In fact, for pure GeTe material, a 100 ns SET pulse is already sufficient to obtain about two orders of magnitude between SET and RESET resistance values. To obtain such a resistance contrast in GeTeC4% a 200 ns pulse width is needed, while for GeTeC10% even a 500 ns pulse width is not sufficient. To better explore the characteristics, in Figure 2.14 we plot the minimum SET resistance value obtained from Figure 2.13 for each programming time and for each alloy. While for GeTe-based memories a 200 ns pulse is already sufficient to bring the cell to a minimum resistance value, GeTeC4% and GeTeC10% require more time to reach a full SET state. Then, it is clear that in GeTeC, for a given pulse time, the minimum resistance value achievable

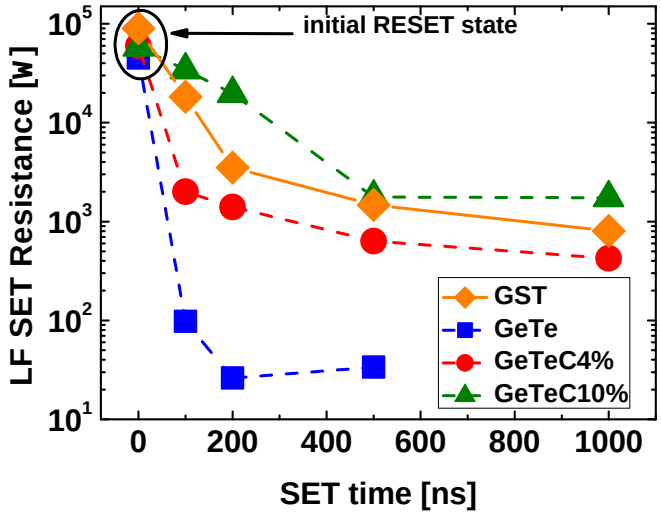


Figure 2.14: LF SET state resistance as a function of SET time for GST, GeTe, GeTeC4% and GeTeC10% PCM. 100 ns, 200 ns, 500 ns and 1 μs SET pulses are applied to the cells and then resistance is measured at LF. The point correspondent to 0 ns reports the initial resistance value of the PCM in RESET state. Each point is obtained by averaging on about 30 cells.

property	GST	GeTe	GeTeC4%	GeTeC10%
T_C [°C]	145	180	290	340
SET time (10x) [ns] (rough) estimation	150	30	100	300

Table 2.1: Summary of GST, GeTe, GeTeC4% and GeTeC10% characteristics, in terms of crystallization temperature T_C (measured at the condition specified in Figure 2.3, and with GST data from Ref.[Fan09]), and of SET time estimation (a reduction of a factor 10 of amorphous state resistance has been taken as the reference, see Figure 2.14).

increases with carbon doping, confirming that the crystallization dynamics is hampered by a much higher C concentration. Furthermore, GeTeC fully polycrystalline state is characterized by a higher resistivity compared to GeTe, featuring so a narrower resistance window. Nevertheless, GeTeC has SET speed and resistance window directly comparable to those of the reference GST material.

The trade-off between data retention and SET programming performances of the chalcogenide materials investigated is summarized in Table 2.1.

GeTe is characterized by faster programming capabilities, showing also the larger re-

sistance window. GeTeC is slower than GeTe and has a resistance window significantly reduced. Nevertheless, GeTeC SET time and resistance window are comparable to GST ones.

2.5 Conclusions

In this chapter we have presented novel experimental findings about carbon-doped GeTe blanket layers and PCM devices. C doping has a beneficial effect on PCM data retention: PCM devices integrating GeTeC10% can guarantee a 10 years fail temperature of about 127°C. Moreover, C doping reduces fail time dispersion. Furthermore, our data highlight a reduction of both RESET current and power when C is added. In particular, GeTeC10% PCM devices yield about 30% of RESET current reduction in comparison to GST and GeTe ones, which translates in about 50% RESET power decrease. SET operation for GeTeC devices results slower with respect to GeTe ones, although it remains in the hundreds of ns range, featuring GST-like SET program times. GeTeC resistance window is narrower than that of GeTe but results directly comparable to that of GST.
To conclude, both data retention up to 127°C and 30% RESET current reduction indicate GeTeC10% as a promising candidate for both embedded and stand-alone PCM applications.

Chapter 3

Implementation, modeling and characterization of a low-frequency noise experimental setup

3.1 Abstract

This chapter describes the experimental setup for low-frequency noise characterization developed at the *Laboratorio di Strumentazione* of *Università degli Studi di Modena e Reggio Emilia, Dipartimento di Ingegneria dell'Informazione, Modena*. The system has been designed for low-frequency noise measurements on two-terminals solid-state devices. In the following, we implement the instrumentation measurement chain and present an experimental and theoretical study of the setup noise intrinsic sources. Our investigation allows to analytically de-embed the setup of the Device Under Test from the setup intrinsic noise contribution. Furthermore, setup physical limitations, probably due to some resonance effects originated in Low-Noise Amplifier employed, are highlighted and discussed. Then, our analytical model is validated by measurements on test resistors and diodes. Finally, we present low-frequency noise measurements on Phase-Change Memory devices as possible setup application.

3.2 Introduction

This Chapter is organized as follows. In Section 3.3 we briefly discuss the importance of low-frequency noise in solid-state science and engineering. In Section 3.4, the structure and the working principle of the experimental setup is described in detail. Section 3.5

reminds some elements of Fourier's analysis, the mathematical method employed to analyze fluctuating quantities. An in-depth analysis of the two more critical components of the setup, (i.e. the current bias and the Low-Noise Amplifier (LNA)) is presented in Sections 3.6 and 3.7. Section 3.8 describes the cables ad-hoc fabricated for connecting the various setup components. Moreover, an analytical formula to extract the noise contribution of the Device Under Test (DUT) from the overall noise of the whole experimental setup is derived (see Section 3.9). Then, to validate the analytical model, noise measurements collected on resistors and diodes are presented and compared with theory in Section 3.10. Finally, as example of application, in Section 3.11 we show measurement of the low-frequency noise of polycrystalline Phase-Change Memory (PCM) devices and compare our results with recent literature.

3.3 Motivation

The presence of electronic noise processes sets the minimum measurable signals in the electronic systems, thus limiting the signal-to-noise ratio. Electronic noise phenomena affect, in various forms, each kind of electronic device. Among the different types and sources of noise, the low-frequency noise, almost ubiquitous in solid-state system, is a field of primary research interest. Although it is widely accepted that the presence of electronic traps inside materials affects the noise magnitude, conflicting pictures have been proposed to explain its cause [Dut81], and up to today, a unified theory is still missing, strongly motivating further investigations. Moreover, noise in condensed matter has long been recognized as a problem, especially in the field of semiconductor devices [VdZ70]. Because of the strict correlation between noise processes and internal structure of materials, as well as device architectures, noise studies are also known to be valuable sources of information. In fact, low-frequency noise characterization can be considered as a diagnostic tool for quality and reliability of microelectronic devices [Vda94], allowing understanding electronic processes inside materials especially in non-crystalline semiconductors [Wei96][Bet09]. For these reasons, the developing of new and better experimental equipments to accurately perform low-frequency noise characterization on solid-state devices is a subject of special interest for solid-state device physicists and engineers.

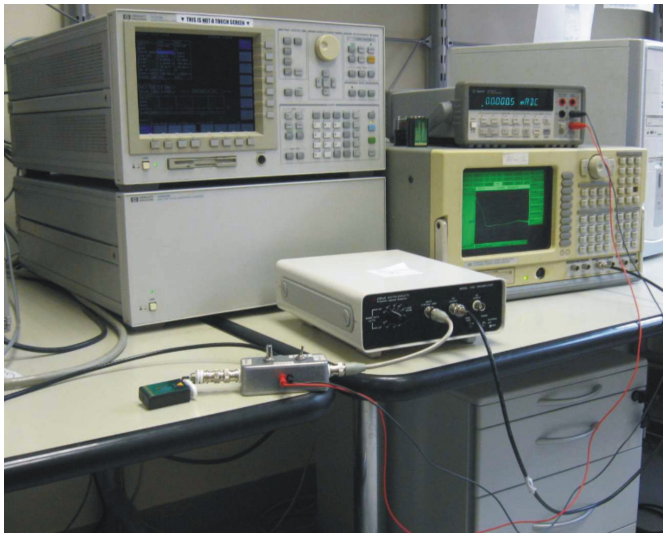


Figure 3.1: Experimental equipment for low-frequency noise characterization developed at the *Laboratorio di Strumentazione* of *Università degli Studi di Modena e Reggio Emilia, Dipartimento di Ingegneria dell'Informazione, Modena*.

3.4 Noise instrumentation

3.4.1 Building Blocks

A picture of the low-frequency noise measurement system is presented in Figure 3.1. The main setup building blocks, depicted in Figure 3.2, are: i) a homemade DC current generator, capable of providing a stable bias current in the [1 μA $\div$ 120 μA] range; ii) the *EG&G 5182* Low-Noise Amplifier (LNA) and iii) the *SRS SR785* Dynamic-Signal Analyzer (DSA).
Furthermore, to get the $I - V$ characteristics of the same devices under noise test, the

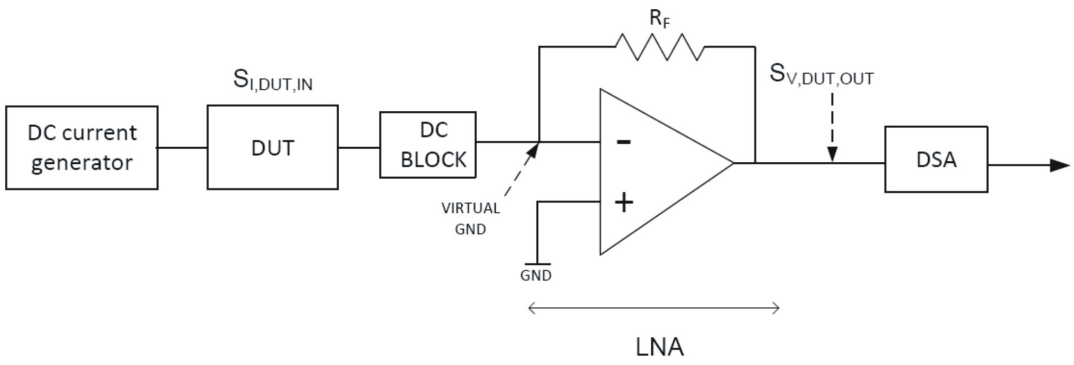


Figure 3.2: Block structure of the low-frequency noise setup.

capability of switching between the noise setup connections and the input channels of a *HP4155B Semiconductor Analyzer* (parameter) has also been implemented by using a homemade coaxial-triaxial interface.

3.4.2 Overview on block operations

The DC homemade current generator biases the two-terminals DUT with a DC current, I_{BIAS}. Due to the physical nature of the DUT, an $i(t)$ time-varying current *noise* signal arises in addition to the DC current quiescent point I_{BIAS}. So, at a given time, the total current flowing through the DUT can be written as $I_{DUT} = I_{BIAS} + i(t)$. Since the goal of the noise characterization is to in-depth analyze the property of the $i(t)$ contribution, a DC-block must be included to filter the I_{BIAS} DC component. Then, to get a suitable resolution of the $i(t)$ quantity, we need to amplify the $i(t)$ signal that, in general, could be very weak. This is accomplished by using the LNA. Finally, the analysis of the amplified $i(t)$ signal in the frequency domain (characterization of magnitude and slope of the noise spectrum) is done by using the DSA.

3.5 Fourier analysis

3.5.1 Root mean square and power spectral density

In this paragraph, we shortly remind the fundamental mathematical quantities that are used in noise analysis. The reader could analyze more in depth the mathematical foundations of the formulae and theorems here presented by referring to any classical text on the theory of signals or on noise theory, such as [VdZ70].
The electronic noise phenomena are stochastic processes described by statistical quantities. Under the hypothesis that a stochastic process is *ergodic*, the statistical properties of the process can be derived from the observation of the time evolution of one single realization of the process. Furthermore, since the electronic noise phenomena are fluctuations of an electrical variable (current or voltage), to estimate the amount of noise in the system it is convenient to calculate the *power* associated to the temporal evolution of a realization of the noise process.
More precisely, a parameter of interest for noise analysis is the *root mean square* (rms)

of a fluctuation function $i(t)$, defined as:

$$\overline{i(t)^2} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} |i(t)|^2 dt, \tag{3.1}$$

where T is the observation time of the signal $i(t)$.
To study quantities that fluctuate, a powerful method is Fourier's analysis. Fourier frequency analysis is generally adopted for noise studies since it is easier to characterize fluctuating signals in the frequency domain rather than in time domain [VdZ70]. Let us derive the mathematical function corresponding to $\overline{i(t)^2}$ in the frequency (f) domain. From Eq.(3.1), expressing $i(t)$ with its Fourier's antitrasform, we get:

$$\overline{i(t)^2} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} |i(t)| \cdot \Big(\frac{1}{2\pi} \int_{-\infty}^{+\infty} |i(\omega)| e^{j\omega t} d\omega\Big) \cdot dt, \tag{3.2}$$

where $\omega = 2\pi f$ is the angular frequency. Equivalently:

$$\overline{i(t)^2} = \lim_{T\to\infty} \frac{1}{T} \int_{-\infty}^{+\infty} |i(\omega)| \cdot \Big(\frac{1}{2\pi} \int_{-T/2}^{T/2} |i(t)| e^{j\omega t} dt\Big) d\omega = \int_{-\infty}^{+\infty} \lim_{T\to\infty} \frac{|i(\omega)|^2}{T} d\omega. \tag{3.3}$$

Defining the *unilateral power spectral density* of $i(t)$, $N_I(\omega)$, as:

$$N_I(\omega) = \lim_{T\to\infty} \frac{|i(\omega)|^2}{T}, \tag{3.4}$$

we get:

$$\overline{i(t)^2} = \int_{-\infty}^{+\infty} N_I(\omega) d\omega. \tag{3.5}$$

If the $i(t)$ signal is real, N_I is an even function of ω, so:

$$\overline{i(t)^2} = 2 \int_{0}^{+\infty} N_I(\omega) d\omega = \int_{0}^{+\infty} S_I(\omega) d\omega, \tag{3.6}$$

where $S_I(\omega)$ is the *bilateral power spectral density* (PSD). According to the Wiener-Kintchine theorem, $S_I(\omega)$ can also be calculated as:

$$S_I(\omega) = 4 \int_{0}^{\infty} \overline{i(t) i(t+\tau)} cos(\omega\tau) d\tau, \tag{3.7}$$

that is, the PSD is equal to the antitrasform of the *autocorrelation function* $R_\tau(\tau)$, which is defined as:

$$R_\tau(\tau) = \overline{i(t)i(t+\tau)} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} i(t)i(t+\tau)dt. \tag{3.8}$$

The PSD function is the main quantity of interest for noise analysis. The DSA instrument measures the autocorrelation function $R_\tau(\tau)$ and calculates Eq.(3.7) by means of a Fast-Fourier Transform (FFT) algorithm. All data and considerations in the following are given by representing the noise functions with their PSD.

3.5.2 Transfer function and correlation in linear systems

Consider a linear system. Given an input signal $X(\omega)$ and an output signal $Y(\omega)$, we can describe the linear system by referring to its transfer function $H(\omega)$ [VdZ70]:

$$Y(\omega) = H(\omega) \cdot X(\omega). \tag{3.9}$$

Switching to the power $X(\omega)^2$ and $Y(\omega)^2$, Eq.(3.9) simply becomes:

$$Y(\omega)^2 = H(\omega)^2 \cdot X(\omega)^2. \tag{3.10}$$

Consider now two noise PSD sources referring to the same linear system. Since they generates from the same physical processes, they can be, in general, *correlated*. According to the theory of signals, two PSD sources, S_I and S_V, in input to a linear system characterized by transfer functions $H_I(\omega)$ and $H_V(\omega)$, respectively, generate a total output noise PSD S_{TOT} given by [VdZ70] (see also Figure 3.3):

$$S_{TOT}(\omega) = |H_I(\omega)|^2 \cdot S_I(\omega) + |H_V(\omega)|^2 \cdot S_V(\omega) + 2\Re\{S_{IV}(\omega) \cdot H_I(\omega) \cdot H_V(\omega)^*\}, \tag{3.11}$$

where S_{IV} is the defined as the *cross-correlation PSD* associated to S_I and S_V sources, and can be written as:

$$S_{IV} = \frac{C_{COR}}{\sqrt{S_I \cdot S_V}}, \tag{3.12}$$

in which the coefficient C_{COR} ϵ ([-1;1]) is often indicated as the *correlation coefficient*.

3.5.3 Working principle of the noise setup

In the last part of this Section, we illustrate the basic working principle of the noise setup, based on the exploitation of Fourier's analysis. In this paragraph, we consider the

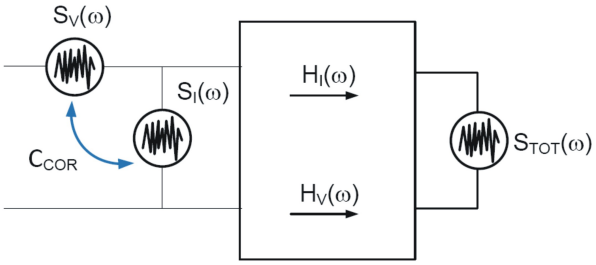


Figure 3.3: Correlation in linear systems.

setup ideal, that is, completely *noiseless*: in other words, we neglect, for the moment, the intrinsic noise setup contribution, considering the DUT the only source of noise. We proceed this way in order to describe the working principle of the setup in a more comprehensive way. Later on this approximation will be removed and the noise intrinsic contribution of the setup quantified.
As already pointed out, for $1/f$ measurements, we exploit Fourier's method to analyze the $i(t)$ signal in the frequency domain representing the PSD of the noise sources. Thus, the goal of the noise measurement setup is acquiring the PSD of the noise. According to the Wiener-Kintchine theorem (i.e. Eq.(3.7)), the PSD $S_{I,DUT,IN}$ associated to the $i(t)$ current signal can be written as:

$$S_{I,DUT,IN} = 4 \int_0^\infty \overline{i(t)i(t+\tau)} cos(\omega\tau) d\tau. \tag{3.13}$$

In order to obtain $S_{I,DUT,IN}$ applying Eq.(3.13), we need an instrument able to sample the $i(t)$ signal and calculate the FFT. This is what the DSA does.
However, the LNA is a transimpedance amplifier. This means that the noise signal at the LNA input, $i(t)$, corresponding to $S_{I,DUT,IN}$, is actually converted in a voltage signal $v(t)$ at the LNA output, to which corresponds a PSD given by:

$$S_{V,DUT,OUT} = 4 \int_0^\infty \overline{v(t)v(t+\tau)} cos(\omega\tau) d\tau, \tag{3.14}$$

that is the one *actually* measured by the DSA, directly connected to the amplifier output port (see Figure 3.2). In Eq.(3.14), $v(t) = G_{AC} \cdot i(t)$, where G_{AC} is the AC gain of the LNA. Therefore, $S_{V,DUT,OUT} = {G_{AC}}^2 \cdot S_{I,DUT,IN}$, and we can calculate $S_{I,DUT,IN}$ from the measured $S_{V,DUT,OUT}$ as:

$$S_{I,DUT,IN} = \frac{S_{V,DUT,OUT}}{{G_{AC}}^2}. \tag{3.15}$$

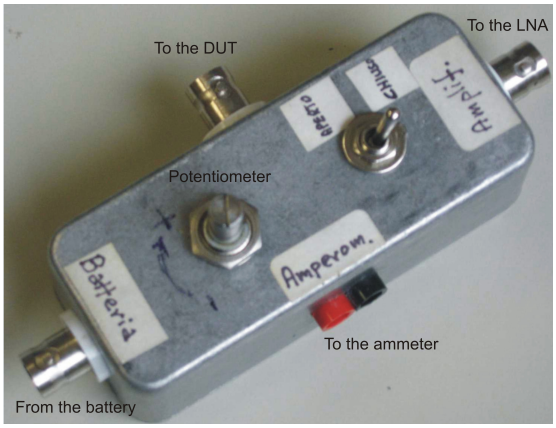


Figure 3.4: Picture of the homemade current bias circuit in its metallic shield.

3.6 Bias circuit

A picture of the homemade current bias circuit in its metallic shield is represented in Figure 3.4. The circuit to generate the DC bias current, I_{BIAS}, is shown in Figure 3.5. In order to avoid any disturb from the power line (50 Hz), the bias circuit is battery-powered with a rechargeable electrochemical cell providing a voltage $V0$=9 V. $V0$ drops on two resistances: a fixed 1 kΩ resistance (R) and a variable resistance ($R_P =$ 10 kΩ). R_P is physically made by a constantan potentiometer with a low-noise sliding contact. Adjusting the potentiometer contact allows to regulate the I_{BIAS} value. The $C1$=15pF capacitor is useful to filter the high-frequency harmonics of the white noise induced by the potentiometer sliding contact. An ammeter (A in the figure) is used to monitor the current flowing through the circuit and to let the user adjusting in real time the desired I_{BIAS}. Since the ammeter could be a significant source of noise, it is very important to disconnect the ammeter during the noise measurement. To this aim, a switch is inserted in the circuit. The user can regulate the bias current with the switch opened (with all the current flowing through the ammeter), then close the circuit (with no current flowing through the ammeter) and, *eventually*, physically remove the ammeter connector cables before getting the noise spectrum [1]. The R_{OUT}=66.3kΩ resistance establishes the output resistance of the bias circuit. A high R_{OUT} value is needed in order to make the I_{BIAS} value as well as possible independent by R_{DUT}.

The representation of I_{BIAS} as a function of R_{DUT} for three different combinations of the potentiometric resistances is given in Figure 3.6. Considering, for the sake

[1]The user must remove the ammeter cable connections when the circuit is closed, otherwise a displacement current would generate in the circuit and probably destroy the DUT due to the high potential difference existing between the cables just after the disconnection.

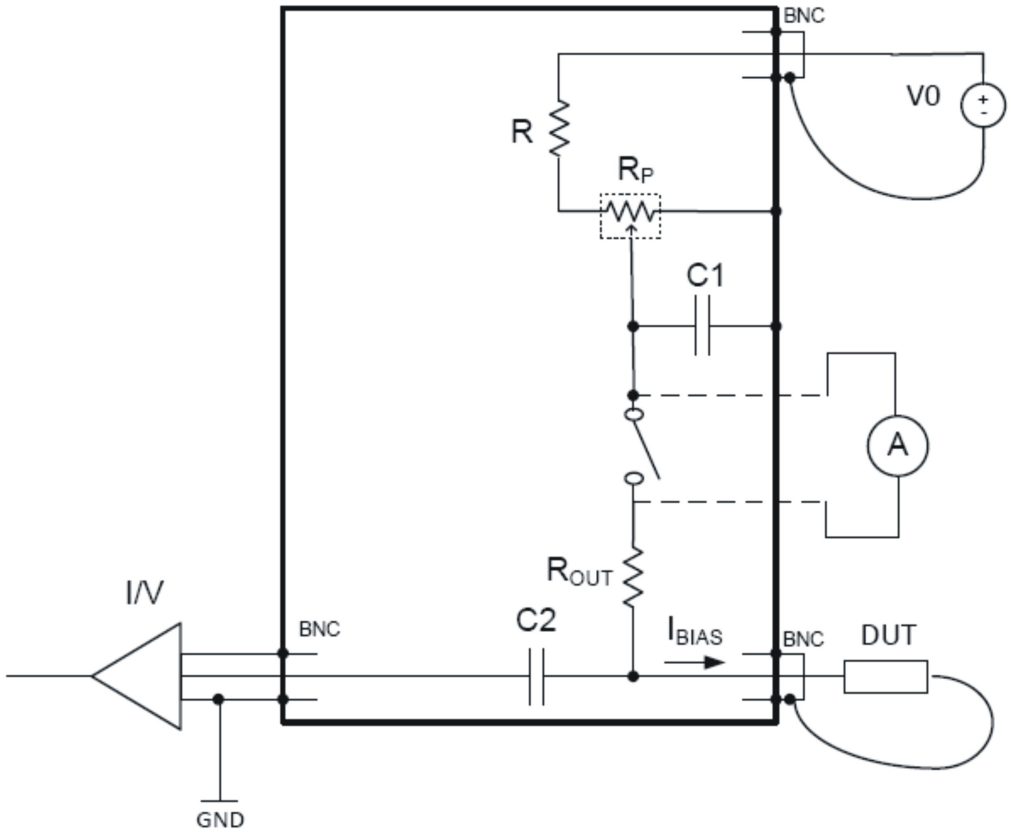


Figure 3.5: Circuit used to generate the DC I_{BIAS} current to bias the DUT.

of simplicity, to split the variable R_P resistance in two equal fractions $R_P/2$ (see Figure 3.7), we have:

$$I_{BIAS} = V0 \cdot \frac{(R_{OUT} + R_{DUT})||R_P/2}{(R_{OUT} + R_{DUT})||R_P/2 + R + R_P/2} \cdot \frac{1}{R_{OUT} + R_{DUT}}. \qquad (3.16)$$

To study the effect of $V0$ and R_{OUT} on I_{BIAS}, we calculate Eq.(3.16) for different combination of V0 and R_{OUT}. Figure 3.8 shows that, in principle, to increase I_{BIAS} we should increase the voltage delivered by the battery, but this worsens the flatness of the current response (compare black and red curves); on the other hand, increasing R_{OUT} increases the flatness of the I_{BIAS}-R_{DUT} characteristics, but limits the bias current value (consider black and dark blue curves). The $V0$ and R_{OUT} chosen values are the result of a trade-off between deliverable current and response flatness.

To conclude the description of the bias circuit, consider the de-coupling capacitance $C2$=100μF, indicated as *DC block* in Figure 3.2. This capacitance is needed to make all the DC current flowing through the DUT. In this way, I_{BIAS} comes back to the negative pole of the battery flowing through the ground wire. On the other hand, the $i(t)$ AC

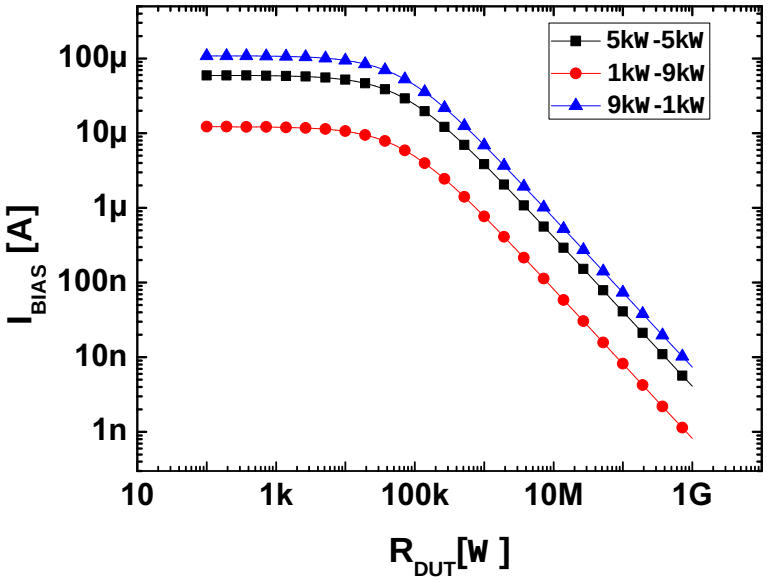


Figure 3.6: I_{BIAS} as a function of R_{DUT} for different combination of the potentiometric resistance R_P (indicated in the legend).

signal generated in the DUT (that is the noise, the quantity we wish to amplify) directly flows towards the I/V amplifier and does not come back to the bias circuit: considering in fact even the lowest frequency of f=1 Hz, the impedance of $C2$ is $1/(2\pi \cdot f \cdot C2)$=1.59 k$\Omega$ $<<$ R_{OUT}.

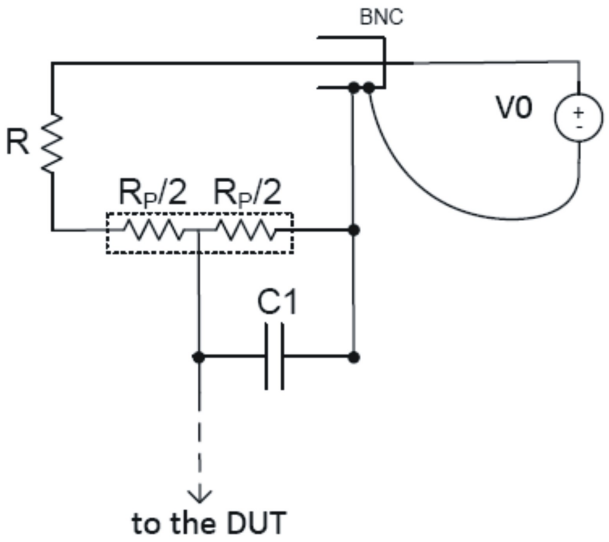


Figure 3.7: Split of the potentiometer resistance and electrical scheme used to calculate Eq.(3.16).

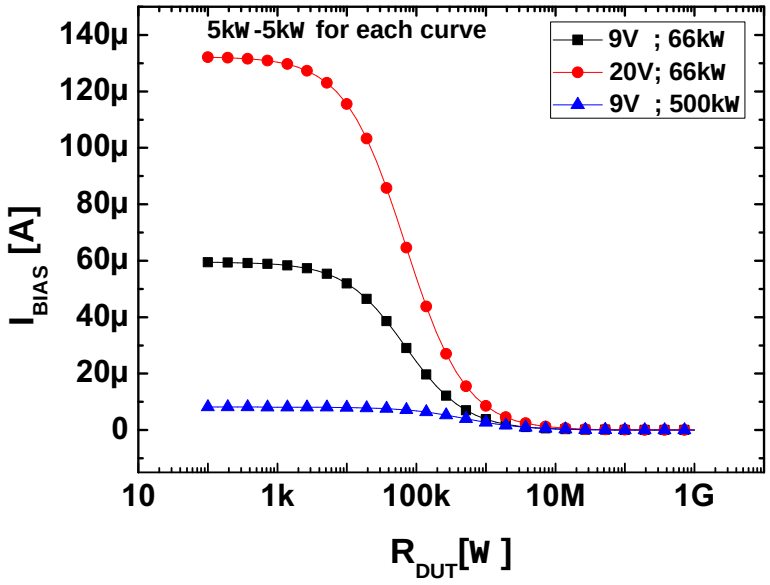


Figure 3.8: I_{BIAS} for different combination of $V0$ and R_{OUT} (see legend). All the curves refer to the case in which the potentiometer resistance R_P is split in two equal $R_P/2 = 5\text{k}\Omega$.

3.7 LNA

The LNA is of fundamental importance for the noise measurement, fixing the maximum measurement bandwidth.

As shown in the following, the LNA intrinsic noise is the dominant contribution of the setup noise. For this reason, it should be carefully examined in order to establish the noise floor of the apparatus.

Taking into account the 3dB bandwidth B_{-3dB} of the amplifier and the maximum DC current $I_{DC,MAX}$ that can be provided to its input port, allows us to make the LNA operating in the linear region. However, note that the presence of the DC block $C2$ removes all the limitations concerning the maximum DC current flowing through the input port of the LNA. The amplifier can provide 5 different AC gain, G_{AC}: 10^5, 10^6, 10^7, 10^8 and 10^8 low-noise. To each G_{AC} are associated a bandwidth, an input resistances R_{IN}, an intrinsic noise level and a maximum DC current. The datasheet parameters as a function of G_{AC} are listed in Table 3.1, where the input resistance value $R_{IN,@10kHz}$ refers to the R_{IN} value at 10kHz.

G_{AC}	B_{-3dB}	$R_{IN,@10kHz}$	$I_{DC,MAX}$
$10^5\Omega$	500 kHz	1 Ω	9mA
$10^6\Omega$	500 kHz	10 Ω	900μA
$10^7\Omega$	200 kHz	$1 \cdot 10^3\Omega$	9μA
$10^8\Omega$	20 kHz	$8 \cdot 10^3\Omega$	900nA
$10^8\Omega$ (low-noise)	10 kHz	$40 \cdot 10^3\Omega$	90nA

Table 3.1: LNA parameters as a function of G_{AC} [from *EG&G 5182* datasheet].

3.8 Connections

To connect the instruments we have used BNC cables, and an extra connection interface has also been realized. To connect the probe station (and so the DUT) to the DC bias current source, the signals coming from the two probes are collected by two different BNC cables (named 1 and 2, see Figure 3.9) onto the probe station metallic cage. They are then assembled in a single BNC (named BNC 3 in the figure) inside a homemade metallic box: the top electrode contact, coming from the core of the BNC 1, is connected to the central core of the BNC 3; the bottom electrode contact, coming from the core of the BNC 2, is connected to the metallic shield of the BNC 3.
Besides, the metallic shield of the BNC 3 is connected to the instrument GND (of the LNA or of the parameter), that acts as the general GND of the experimental setup (see also Figure 3.2).
Furthermore, another homemade metallic box (see Figure 3.10) provides the interface from coaxial output (BNC 3) to triaxial output. In this way, the experimenter can use the same BNC cable (BNC 3), coming from the probe station interface, both for noise measurements (the current bias circuit needs a coaxial input, see Figure 3.4), and for $I-V$ measurements (the parameter needs two triaxial inputs), by simply switching from the current bias circuit input to the metallic box ones.
Figure 3.11 is a schematic of the connection system employed.

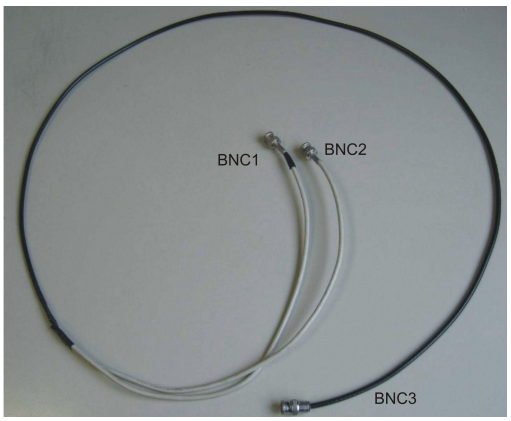


Figure 3.9: Homemade cable to collect in a single BNC (BNC 3) the top electrode signal (from the core of BNC 1, to the core of BNC 3) and the bottom electrode signal (from the core of BNC 2, to the metallic shield of BNC 3).

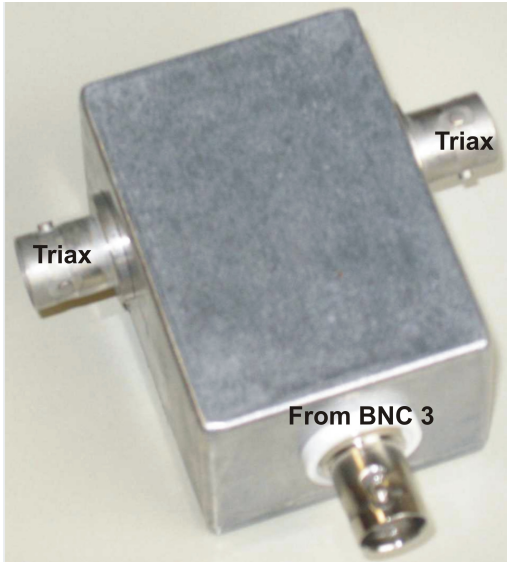


Figure 3.10: Metallic box to connect the BNC 3 directly to the parameter.

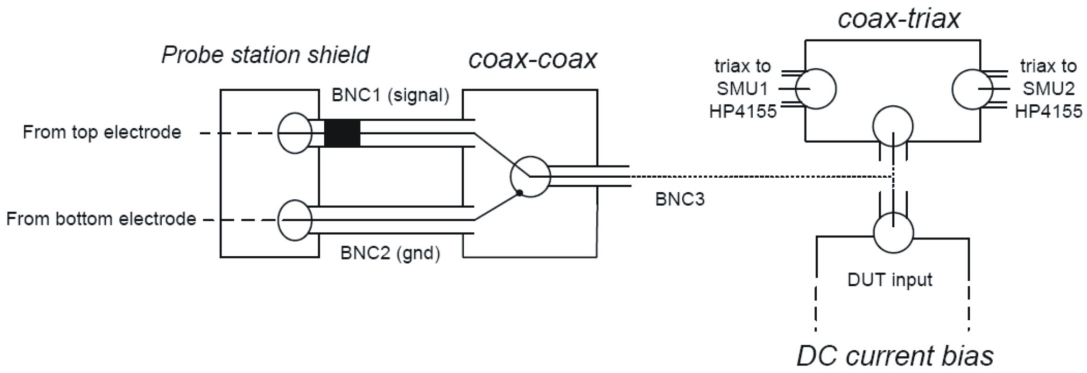


Figure 3.11: System connections employed. The signals, coming from the top and the bottom electrodes of the DUT place inside the probe station, are collected on the probe station metallic shield by BNC1 and BNC2. The two BNCs are assembled in a single BNC3 using a homemade coax-coax metallic box. BNC3 can either be plugged in the input port of the homemade coax-triax metallic box, which provides the connection to the Source-Monitor Units (SMU) of HP4155 (for $I-V$ measurement), or in the DUT terminal of the DC current bias (for noise measurement).

3.9 Modeling and characterization of the setup noise sources

In order to perform a reliable characterization of the noise of the DUT and compare measurements carried out on different equipments, it is very important to model and characterize the intrinsic setup noise contribution. In this way, we can de-embed from the experimental data the setup noise floor and obtain the effective noise signal due to the DUT only. In this Section, we develop an analytical formula that accounts for the noise generated by the whole system (i.e. DUT+experimental setup) and allows to calculate the contribution of each noise source.

3.9.1 Setup equivalent noise circuit

DC bias current source

To compute the noise contribution due to the DC current generator, we calculate the equivalent resistance of the current bias circuit seen from the transimpedance input port (i.e. Thévenin equivalent resistance). We consider $C1$ as an open circuit, since even at relatively high frequency for low-frequency noise measurements such as 10

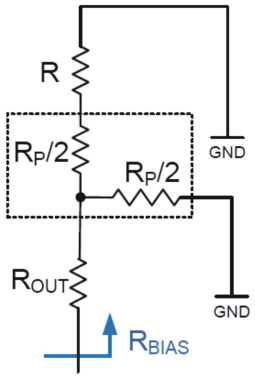


Figure 3.12: Thévenin equivalent circuit of the current bias used to calculate R_{BIAS}.

kHz, the impedance of $C1$ is very high: $\sim 1M\Omega$. Then, we suppose the potentiometer noiseless and, for the sake of simplicity, we consider R_P split in two equal parts $R_P/2$. In this way the equivalent resistance of the current bias circuit is $R_{BIAS} = R_{OUT} + R_P/2||(R_P/2 + R) = 69k\Omega$ (see Figure 3.12). In case of R_P split in a 9kΩ plus a 1kΩ resistors, R_{BIAS} is equal to a similar value of 67kΩ. So, the noise current PSD associated to R_{BIAS} is approximately always given by:

$$S_{I,BIAS} = \frac{4K_BT}{R_{BIAS}} \sim 10^{-25} A^2/Hz \tag{3.17}$$

where K_B is the Boltzmann constant ($\sim 1.38 \cdot 10^{-23} J/K$) and T is the temperature (in K). As it will become clearer in the following by comparison with the other noise contributions, this value is relatively low. This is a beneficial consequence due to the employment of a current generator (that has a high output impedance R_{BIAS}, and so a low $S_{I,BIAS}$) instead of using a voltage generator, characterized by lower output impedance, and so by a higher $S_{I,BIAS}$.

LNA circuit

To model the intrinsic noise contribution of the LNA, we apply a well-known mathematical technique. The method consists in replacing the noise sources, physically *inside* the amplifier, with two mathematical devices that capture the noise behavior of the LNA but that are, from a circuit point of view, placed *outside* and at the input of the LNA. Gathering the noise contribution of the amplifier using two external generators allow us to consider the transimpedance ideal, i.e. noiseless. The two noise generators are a current noise generator $S_{I,LNA}$ and a voltage noise generator $S_{V,LNA}$ placed in parallel

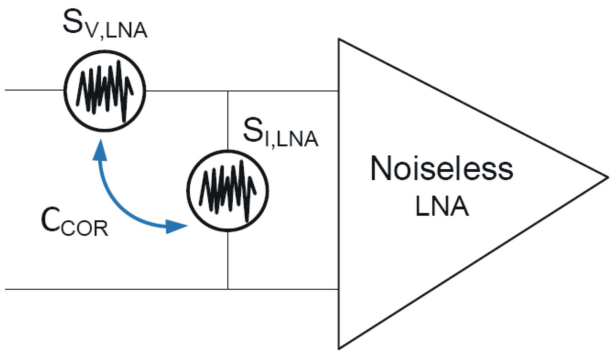


Figure 3.13: LNA equivalent noise circuit. $S_{V,LNA}$ and $S_{I,LNA}$ are in general correlated by a correlation coefficient C_{COR}.

and in series, respectively, to the input port of the transimpedance amplifier. In general, the two generators are not independent each other but exhibit a correlation coefficient, as depicted in Figure 3.13.

Whole system circuit

The equivalent noise circuit of the whole setup is displayed in Figure 3.14. There are 4 noise generators: the one associated to the DUT, $S_{I,DUT}$, the one associated to the DC current generator $S_{I,BIAS}$, and the two associated to the LNA, indicated as $S_{V,LNA}$ and $S_{I,LNA}$. To calculate the overall noise of the system, we singularly compute the effect of $S_{I,DUT}$, $S_{I,BIAS}$, $S_{V,LNA}$, and $S_{I,LNA}$ and sum their contributions; in other words we apply the superposition principle[2]. Considering the equivalent generators of $S_{I,DUT}$, $S_{I,BIAS}$, $S_{V,LNA}$ and $S_{I,LNA}$ in the time domain, named i_{DUT}, i_{BIAS}, e_V, and e_I, respectively, leads to the analysis of the circuits shown in Figure 3.15. The noise currents generated by the three generators flowing through the input resistance of the LNA, R_{IN}, are indicated as $i_{IN,DUT}$, $i_{IN,BIAS}$, $i_{IN,V,LNA}$, and $i_{IN,I,LNA}$, respectively. They can be calculated as follows:

$$i_{IN,DUT} = i_{DUT}\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}, \tag{3.18}$$

$$i_{IN,BIAS} = i_{BIAS}\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}, \tag{3.19}$$

[2]This hypothesis is justified by the fact that the noise analysis is a small signal analysis and that, for small signal analysis, the LNA has a linear transfer function. Obviously, to satisfy the linear transfer function condition it must be, for a given G_{AC}: $I_{BIAS} \leq I_{DC,MAX}$ and $f \leq B_{-3dB}$, see Table 3.1.

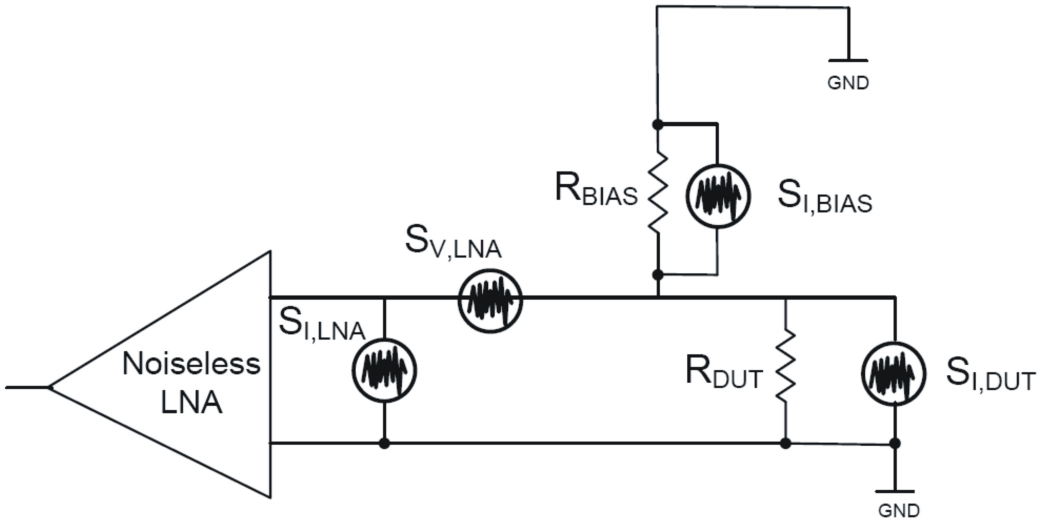


Figure 3.14: Schematics of the setup noise contributions (frequency domain) due to DUT ($S_{I,DUT}$), current bias ($S_{I,BIAS}$), LNA voltage noise ($S_{V,LNA}$), and LNA current noise ($S_{I,LNA}$).

$$i_{IN,V,LNA} = \frac{e_V}{(R_{DUT}||R_{BIAS}) + R_{IN}}, \tag{3.20}$$

$$i_{IN,I,LNA} = e_i \frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}. \tag{3.21}$$

In the frequency domain, according to the transfer function theory, see Eq.(3.10), the corresponding power spectral densities are as the follows:

$$S_{IN,DUT} = S_{I,DUT} \left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}} \right]^2, \tag{3.22}$$

$$S_{IN,BIAS} = S_{I,BIAS} \left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}} \right]^2, \tag{3.23}$$

$$S_{IN,V,LNA} = \frac{S_{V,LNA}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2}, \tag{3.24}$$

$$S_{IN,I,LNA} = S_{I,LNA} \left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}} \right]^2, \tag{3.25}$$

where $S_{IN,DUT}$, $S_{IN,BIAS}$, $S_{IN,V,LNA}$ and $S_{IN,I,LNA}$ are the noise current PSD flowing through R_{IN} corresponding to $i_{IN,DUT}$, $i_{IN,BIAS}$, $i_{IN,V,LNA}$ and $i_{IN,I,LNA}$, respectively. Then, since the current generator $S_{I,LNA}$ and the voltage generator $S_{V,LNA}$ model physical processes referring to the same components (the ones inside the LNA), in

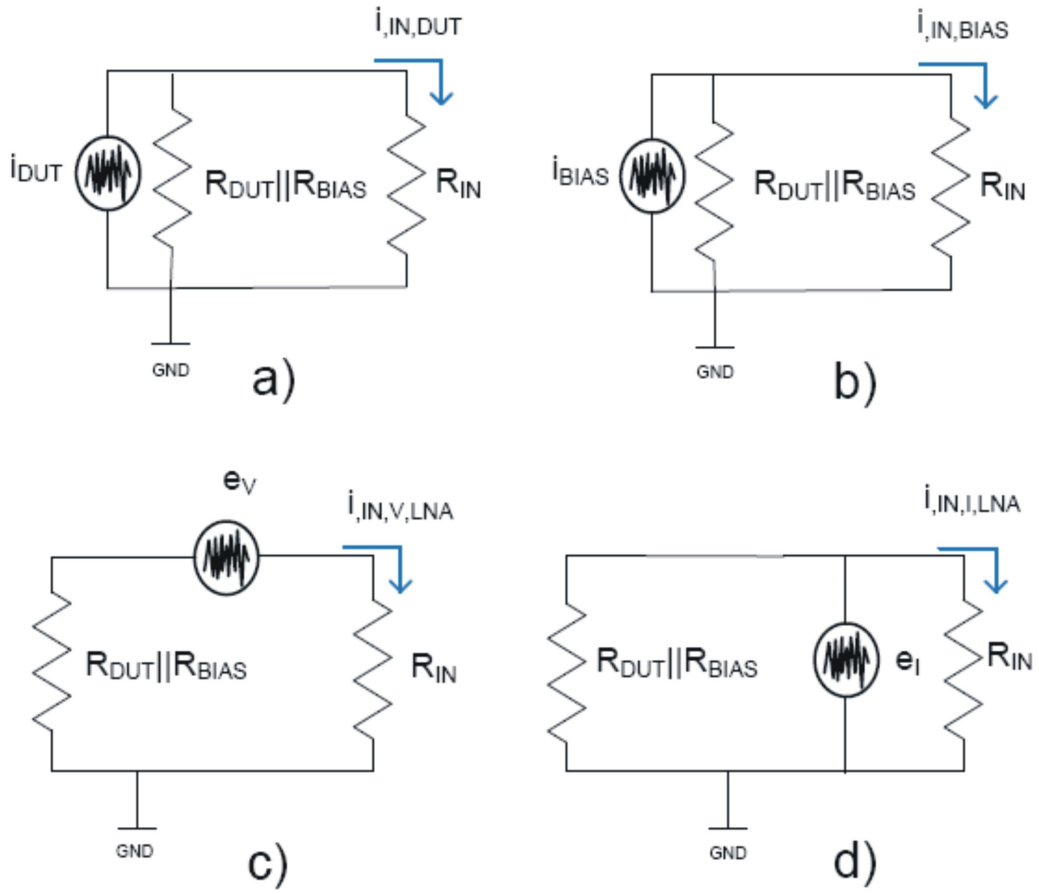


Figure 3.15: Schematics of the setup noise contributions (time domain) due to (a) DUT, (b) current bias, (c) LNA voltage noise and (d) LNA current noise.

general, they can be correlated by a correlation coefficient C_{COR} ϵ ([-1;1]), such that (see Eq.(3.12)):

$$S_{IV,LNA} = \frac{C_{COR}}{\sqrt{S_{I,LNA} \cdot S_{V,LNA}}}, \tag{3.26}$$

where $S_{IV,LNA}$ is the cross-correlation. Thus, in general, the $S_{IV,LNA}$ noise generator must also be taken under consideration and add to the other noise contributions.
Under hypothesis of linearity, and by applying the transfer function theory for correlated

noise sources (i.e. Eq.(3.11)), we obtain a total LNA noise contribution given by:

$$S_{IN,LNA} = S_{IN,V,LNA} + S_{IN,I,LNA} + S_{IN,IV,LNA} = \frac{S_{V,LNA}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2} + \\ + S_{I,LNA}\left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}\right]^2 + \\ + 2 \cdot S_{IV,LNA}\frac{R_{DUT}||R_{BIAS}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2}, \tag{3.27}$$

where $S_{IN,IV,LNA}$ is the current noise flowing through R_{IN} generated by $S_{IV,LNA}$. So, the total current noise that enters into the noiseless LNA input port is given by (sum of DUT, current bias and real LNA contributions):

$$S_{IN,I} = S_{IN,DUT} + S_{IN,BIAS} + S_{IN,LNA} = \\ (S_{I,DUT} + S_{I,BIAS} + S_{I,LNA})\left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}\right]^2 + \\ + \frac{S_{V,LNA}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2} + \\ + 2 \cdot S_{IN,IV,LNA}\frac{R_{DUT}||R_{BIAS}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2}. \tag{3.28}$$

Then, if the LNA is working in the linear region, the DSA measures a noise voltage PSD $S_{OUT,V}$ given by:

$$S_{OUT,V} = S_{IN,I} \cdot {G_{AC}}^2, \tag{3.29}$$

therefore, according to Eq.(3.28), we finally obtain:

$$S_{OUT,V} = S_{IN,I} \cdot {G_{AC}}^2 = \\ \left\{(S_{I,DUT} + S_{I,BIAS} + S_{I,LNA})\left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}\right]^2 + \right. \\ \left. + \frac{S_{V,LNA}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2} + 2 \cdot S_{IN,IV,LNA}\frac{R_{DUT}||R_{BIAS}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2}\right\} \cdot \\ \cdot {G_{AC}}^2. \tag{3.30}$$

Obviously, if the experimental setup would be ideal, that is in case of ideal current generator (i.e. $S_{I,BIAS} \to 0, R_{BIAS} \to \infty$), and of ideal LNA (i.e. $S_{I,LNA} \to 0, S_{V,LNA} \to 0, C = 0$ and $R_{IN} \to 0$), we would have $S_{IN} = S_{I,DUT}$ -see Eq.(3.28)- and therefore the only noise contribution measured by the DSA would be the (amplified) noise of the DUT only: $S_{OUT,V} = S_{I,DUT} \cdot {G_{AC}}^2$ (see Eq.(3.29)).

3.9.2 LNA noise characterization

In Eq.(3.30) there are three unknowns: $S_{I,LNA}$, $S_{V,LNA}$, and $S_{IV,LNA}$.
$S_{I,LNA}$ and $S_{V,LNA}$ can be characterized adopting the procedure illustrated in Figure 3.16. To experimentally measure $S_{I,LNA}$ we disconnect the DUT: in this way, all the $S_{I,LNA}$ noise contribution flows through the R_{IN} resistance and is amplified towards the DSA input port. On the other hand, the whole $S_{V,LNA}$ quantity drops on the open circuit and is not amplified to the output (see Figure 3.16(a)).
Viceversa, to measure $S_{V,LNA}$ we connect a short circuit plug as DUT. In this way, all the $S_{V,LNA}$ noise contribution drops on the R_{IN} resistance and is amplified towards the DSA input port. On the other hand, the whole $S_{I,LNA}$ quantity flows through the short circuit towards GND (see Figure 3.16(b)).
Thus, with the open circuit method, we measure $S_{OUT,V} = S_{IN,I} \cdot {G_{AC}}^2$ -Eq.(3.29)-, with $S_{IN,I} = S_{IN,I,LNA} = S_{I,LNA}$ [3], and therefore we derive $S_{I,LNA}$ as:

$$S_{I,LNA} = \frac{S_{OUT,V}}{{G_{AC}}^2}. \tag{3.31}$$

The measured $S_{I,LNA}$ as a function of G_{AC} is shown in Figure 3.17. To higher G_{AC} is associated a lower noise level.
Using the short circuit method we measure $S_{OUT,V} = S_{IN,I} \cdot {G_{AC}}^2$ -Eq.(3.29)-, with $S_{IN,I} = S_{V,IN,LNA} = S_{V,LNA}/{R_{IN}}^2$, therefore we derive $S_{V,LNA}$ as:

$$S_{V,LNA} = S_{OUT,V} \cdot \frac{{R_{IN}}^2}{{G_{AC}}^2}. \tag{3.32}$$

[3] As shown in Figure 3.16, in these measurements the DUT and the current bias are obviously disconnected.

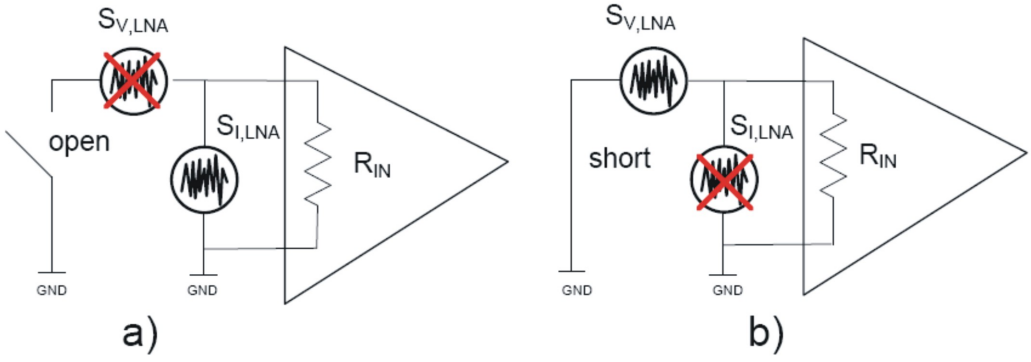


Figure 3.16: Open circuit (a) and short circuit (b) methods to characterize $S_{I,LNA}$ and $S_{V,LNA}$, respectively.

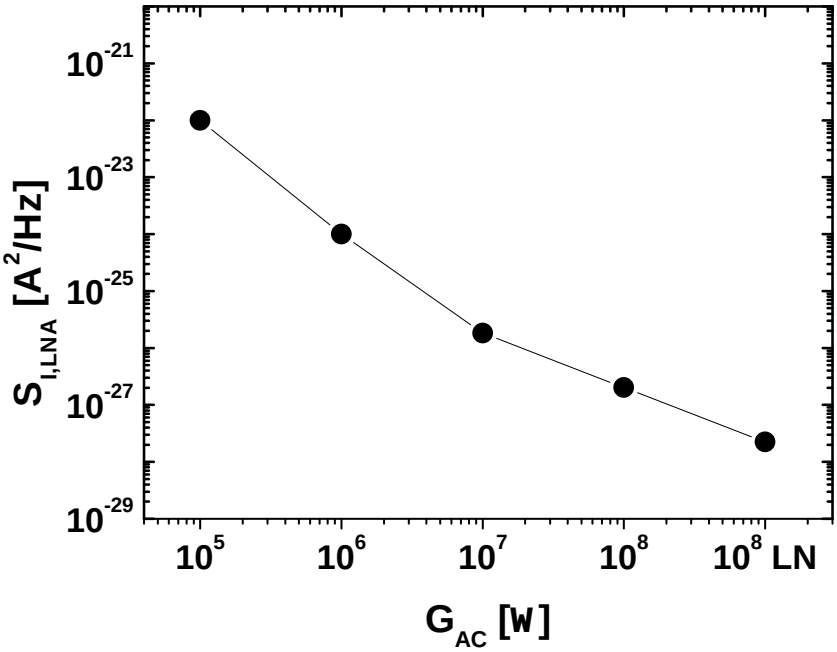


Figure 3.17: Measured $S_{I,LNA}$ as a function of G_{AC}.

The measured $S_{V,LNA}$ as a function of G_{AC} and R_{IN} is represented in Figure 3.19. A linear dependence on a log-log scale between $S_{V,LNA}$ and R_{IN} is evident. To conclude this Section on the LNA noise sources, let us focus on the $S_{IV,LNA}$ term (see Eq.(3.12)). Since there is not a noise source inside the LNA that can be considered *dominant*, this implies that $C_{COR} \to 0$ and then Eq.(3.30) can be further simplified in:

$$S_{OUT,V} = S_{IN,I} \cdot {G_{AC}}^2 = \left\{ (S_{I,DUT} + S_{I,BIAS} + S_{I,LNA}) \left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}} \right]^2 + \right.$$
$$\left. + \frac{S_{V,LNA}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2} \right\} \cdot {G_{AC}}^2. \tag{3.33}$$

Therefore, we can finally derive $S_{I,DUT}$ from the measured $S_{OUT,V}$ as:

$$\boxed{S_{I,DUT} = \frac{S_{OUT,V}}{{G_{AC}}^2} \cdot \left[\frac{(R_{DUT}||R_{BIAS}) + R_{IN}}{R_{DUT}||R_{BIAS}} \right]^2 - S_{I,BIAS} - S_{I,LNA} - \frac{S_{V,LNA}}{(R_{DUT}||R_{BIAS})^2}}. \tag{3.34}$$

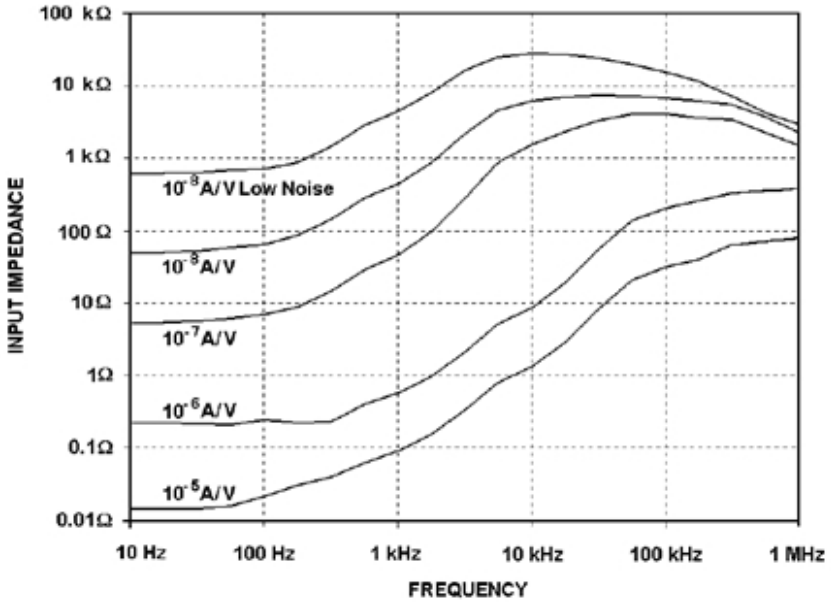


Figure 3.18: LNA input impedance (resistance) R_{IN} as a function of frequency f and sensitivity $S_{AC} = {G_{AC}}^{-1}$ [from *EG&G 5182* datasheet].

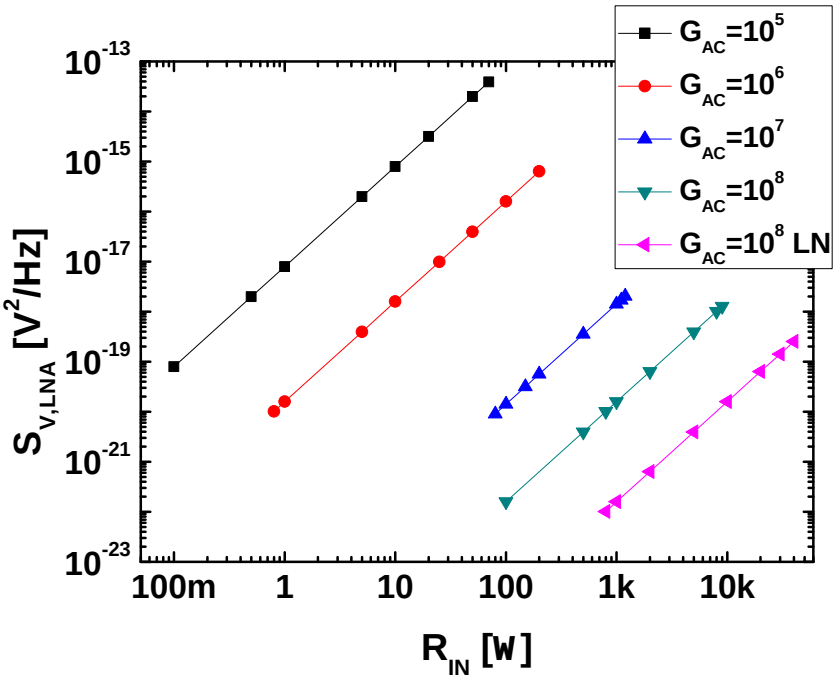


Figure 3.19: Measured $S_{V,LNA}$ as a function of R_{IN} for different values of G_{AC}.

3.10 Setup experimental validation

In this Section, in order to validate our setup modeling procedure and the characterization system operation, we perform noise measurements on DUT having a well known noise behavior: resistors and semiconductor diodes in particular.
In Section (3.10.1) we analyze the response of the noise system collecting the magnitudes of noise spectra $S_{OUT,V}$ of different resistors for different G_{AC}. These measurements are compared with our analytical model of Eq.(3.33). Emphasis is on the the analysis of the noise contribution of each setup component and on non-ideal effects of the LNA.
Section (3.10.2) shows noise spectra as a function of frequency for resistances and diodes. Theoretical $S_{I,DUT}$ are compared with Eq.(3.34) allowing to calculate $S_{I,DUT}$ by de-embedding the noise setup contribution according to our model.

3.10.1 Analysis of different noise source and LNA response

Figures 3.20, 3.21, 3.22, 3.23, and 3.24 show the current noise PSD measured using, as DUT, resistors of variable resistance R_{DUT}, for the different values of G_{AC}, $10^5\Omega$, $10^6\Omega$, $10^7\Omega$, $10^8\Omega$ and $10^8\Omega$ low-noise, respectively. In each graph, $S_{OUT,V}$ is obtained applying Eq.(3.33), while $S_{I,DUT}(out)$, $S_{I,BIAS}(out)$, $S_{I,LNA}(out)$ and $S_{V,LNA}(out)$ are the contributions of DUT, DC current bias, LNA current noise PSD and LNA voltage noise PSD referred to the output of the measurement chain, i.e., according to Eq.(3.33):

$$\begin{aligned}
S_{I,DUT}(out) &= S_{I,DUT} \cdot \left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}\right]^2 \cdot {G_{AC}}^2; \\
S_{I,BIAS}(out) &= S_{I,BIAS} \cdot \left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}\right]^2 \cdot {G_{AC}}^2; \\
S_{I,LNA}(out) &= S_{I,LNA} \cdot \left[\frac{R_{DUT}||R_{BIAS}}{(R_{DUT}||R_{BIAS}) + R_{IN}}\right]^2 \cdot {G_{AC}}^2; \\
S_{V,LNA}(out) &= \frac{S_{V,LNA}}{[(R_{DUT}||R_{BIAS}) + R_{IN}]^2} \cdot {G_{AC}}^2.
\end{aligned} \tag{3.35}$$

In this case, the DUT current noise PSD is given by the well known formula of resistors current noise PSD formula [VdZ70]:

$$S_{I,DUT} = \frac{4 \cdot K_B \cdot T}{R_{DUT}}. \tag{3.36}$$

The R_{IN}, $S_{V,LNA}$ and $S_{I,LNA}$ parameters used in the calculations are listed in Table 3.2. It is worth considering that both R_{IN} and $S_{V,LNA}$ are treated, for the sake of simplicity,

G_{AC}	R_{IN}	$S_{V,LNA}$	$S_{I,LNA}$
$10^5\Omega$	$1\ \Omega$	$2 \cdot 10^{-23}$ V^2/Hz	$1 \cdot 10^{-17}$ A^2/Hz
$10^6\Omega$	$10\ \Omega$	$1 \cdot 10^{-24}$ V^2/Hz	$1 \cdot 10^{-18}$ A^2/Hz
$10^7\Omega$	$1 \cdot 10^3\Omega$	$1.8 \cdot 10^{-26}$ V^2/Hz	$1 \cdot 10^{-18}$ A^2/Hz
$10^8\Omega$	$8 \cdot 10^3\Omega$	$2 \cdot 2 \cdot 10^{-27}$ V^2/Hz	$7 \cdot 10^{-19}$ A^2/Hz
$10^8\Omega$ (low-noise)	$40 \cdot 10^3\Omega$	$2.25 \cdot 10^{-28}$ V^2/Hz	$1.5 \cdot 10^{-19}$ A^2/Hz

Table 3.2: R_{IN}, $S_{I,LNA}$ and $S_{V,LNA}$ parameters used to calculate Eq.(3.33) in Figures 3.20-3.24 as a function of G_{AC}.

as constants. The chosen R_{IN} values are the ones referring to the frequency of 10 kHz (see Figure 3.18), and the $S_{V,LNA}$ parameters are the R_{IN}-corresponding of Figure 3.19[4].

For $G_{AC} = 10^5\Omega$ (Figure 3.20), the analytical noise model fits very well the experimental data. For the other G_{AC} values, the model does not provide the same agreement with experimental data. The fit is very good only for very low or very high DUT resistances, that is, where we get close to the ideal open circuit and close circuit conditions, respectively. At intermediate resistance values, the analytical model underestimates the noise floor of the setup for $G_{AC} = 10^6, 10^7$ and 10^8; the opposite, that is the measurements are overestimated, in case of $G_{AC} = 10^8$ low-noise. $G_{AC} = 10^8$ low-noise corresponds to a very low setup-induced noise, probably due to the fact the the DC working point of the LNA transistors is lowered . A possible explanation of the illustrated behavior is the following: the LNA is a transimpedance amplifier, it means that it is designed to receive a current from a current generator, that has a high output impedance. For this reason, it works better when the resistance of the DUT is high. Moreover, the noise behavior of the system is determined by the presence of the dominant pole of the LNA, which depends on the G_{AC} value (that is, on the R_F value). For intermediate R_{DUT} (i.e. not so low to be considered as short circuits), the dominant pole of the amplifier is not well compensated, leading to an actual noise behavior of the LNA that differs from the one predicted by the model due to some resonance effect.
It is worth noting that, for $G_{AC} = 10^6\Omega, 10^7\Omega, 10^8\Omega$ and $10^8\Omega$ low-noise, *only* at intermediate R_{DUT} values the $S_{I,DUT}$ contribution dominates the noise response. Then, for $G_{AC} = 10^5$ $S_{I,DUT}$ is never dominating.

[4]The R_{IN} values are the same indicated as $R_{IN,10kHz}$ in Table 3.1; the $S_{I,LNA}$ values are the ones displayed in Figure 3.17.

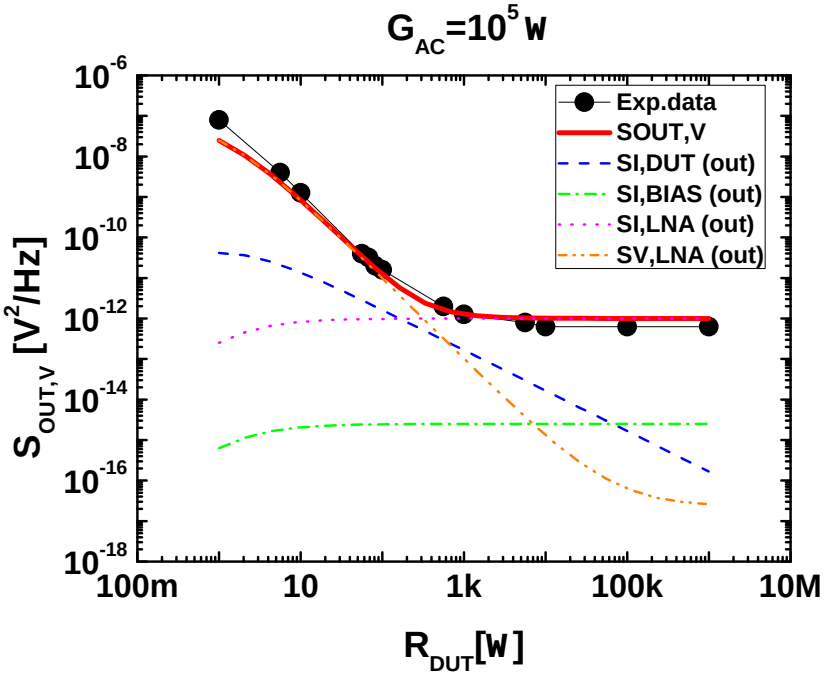


Figure 3.20: Lines: $S_{OUT,V}$, $S_{I,DUT}(out)$, $S_{I,BIAS}(out)$, $S_{I,LNA}(out)$ and $S_{V,LNA}(out)$ as a function of R_{DUT}, calculated using Eq.(3.33) and Eq.(3.35), for $G_{AC} = 10^5\Omega$. Dots refer to experimental $S_{OUT,V}$ data.

Furthermore, for each G_{AC}, the noise floor at lower R_{DUT} is mainly given by $S_{V,LNA}(out)$. On the other hand, at higher R_{DUT}, the noise floor results determined by $S_{I,LNA}$ at $G_{AC} = 10^5\Omega$ and $10^6\Omega$, while, for the other G_{AC}, the most importance contribution is given by $S_{I,BIAS}(out)$.
Importantly, by carefully analyzing the noise response at each G_{AC}, one realizes that for device resistances in the range $10\ \Omega < R_{DUT} < 70\ \Omega$ there is not a G_{AC} value for which our model fits the experimental data. For this reason, since these effects originated by the LNA unproper response, we argue that, using the LNA *EG&G 5182*, it is not possible to make a *reliable* measure of the DUT noise in the above resistance range. This conclusion calls for a customized design of a transimpedance amplifier for these R_{DUT} values.

3.10.2 Test of the analytical model

DUT: resistances

The first devices used to test the analytical model of Eq.(3.34) are resistors of R_{DUT}= 1kΩ, 10kΩ and 100kΩ. To be able to control the noise behavior of the measure-

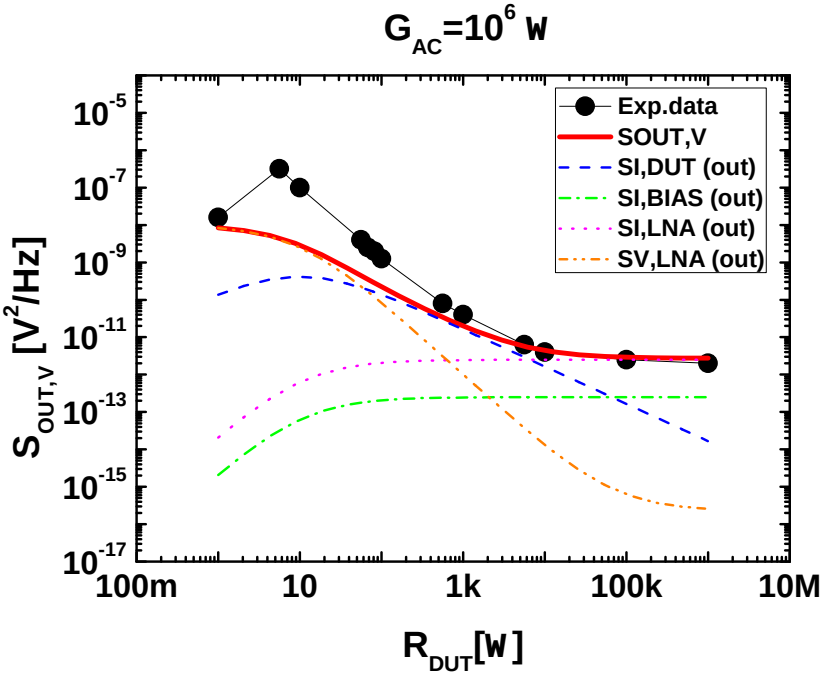


Figure 3.21: Lines: $S_{OUT,V}$, $S_{I,DUT}(out)$, $S_{I,BIAS}(out)$, $S_{I,LNA}(out)$ and $S_{V,LNA}(out)$ as a function of R_{DUT}, calculated using Eq.(3.33) and Eq.(3.35), for $G_{AC} = 10^6\Omega$. Dots refer to experimental $S_{OUT,V}$ data.

ment setup in these tests, we use $G_{AC} = 10^6\Omega$. In this case indeed, within the 1k$\Omega \leq R_{DUT} \leq$ 100kΩ range, the setup noise floor is very well modeled by Eq.(3.33), see Figure 3.21 [5]. In each graph, the analytical $S_{I,DUT}$ calculated from the experimental $S_{V,OUT}$ through Eq.(3.34) are directly compared with $S_{I,DUT}$ theoretical values expressed by Eq.(3.36).

As it appears clear from Figure 3.25, the analytical model agrees very well with the theoretical calculated values, suggesting that, for these parameters, the setup noise contribution is well accounted by our formula, which allows to correctly get the DUT noise contribution. In Figure 3.26 we display the noise spectra for the resistors under test using $G_{AC} = 10^7$. For R_{DUT}=10kΩ and R_{DUT}=100kΩ, that are R_{DUT} values, for which our noise model fit the data (see Figure 3.22), the agreement between theory and model is very good. On the other hand, the spectrum associated to R_{DUT}=1kΩ, for which Eq.(3.33) does not reproduce the data, results to be inappropriate. The PSD

[5] As already pointed out in the chapter, it is very important to choose, for each measurement, an AC gain that does not saturate the LNA (see Table 3.1). This is obviously done for all the measurements that are shown in the next Section: for the given G_{AC} we always check that the condition $I_{BIAS} < I_{DC,MAX}$ is satisfied.

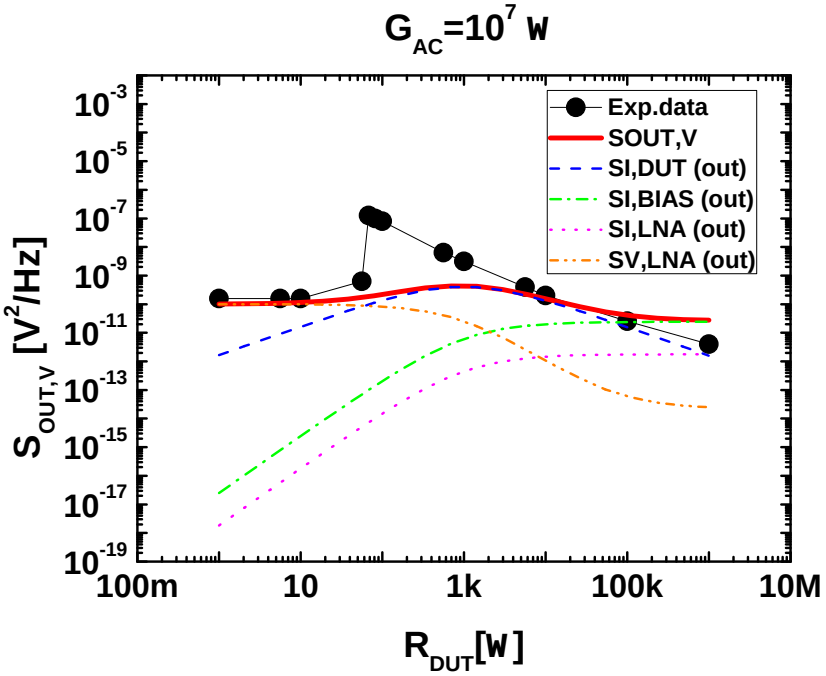


Figure 3.22: Lines: $S_{OUT,V}$, $S_{I,DUT}(out)$, $S_{I,BIAS}(out)$, $S_{I,LNA}(out)$ and $S_{V,LNA}(out)$ as a function of R_{DUT}, calculated using Eq.(3.33) and Eq.(3.35), for $G_{AC} = 10^7\Omega$. Dots refer to experimental $S_{OUT,V}$ data.

appears attenuated at the higher frequency, while a noise spectrum of a resistor should be white (i.e. constant) as a function of frequency. This measurement indicates that, in the intervals where our noise model does not fit well with the experimental data, the behavior of the system is not in accordance with well-established physical laws, suggesting that, in these cases, the behavior of the LNA is somewhat distorted from the nominal expected one. In other words, this experimental finding agrees with the data reported in Figure 3.26. The DUT resistance value of 1kΩ falls indeed in the region where the model does not fit the experimental data.

DUT: diodes

The current noise PSD associated to a semiconductor diode (shot noise) reads as [VdZ70]:

$$S_{I,DUT} = 2 \cdot q \cdot I_D, \tag{3.37}$$

where $q = 1.6 \cdot 10^{-19}$ C is the elementary charge, and I_D is current flowing through the diode, given by [VdZ70]. In Figure 3.27 we display the $I_D - V_D$ characteristics of the semiconductor diode under test. Substituting in Eq.(3.34) the values of $S_{I,DUT}$

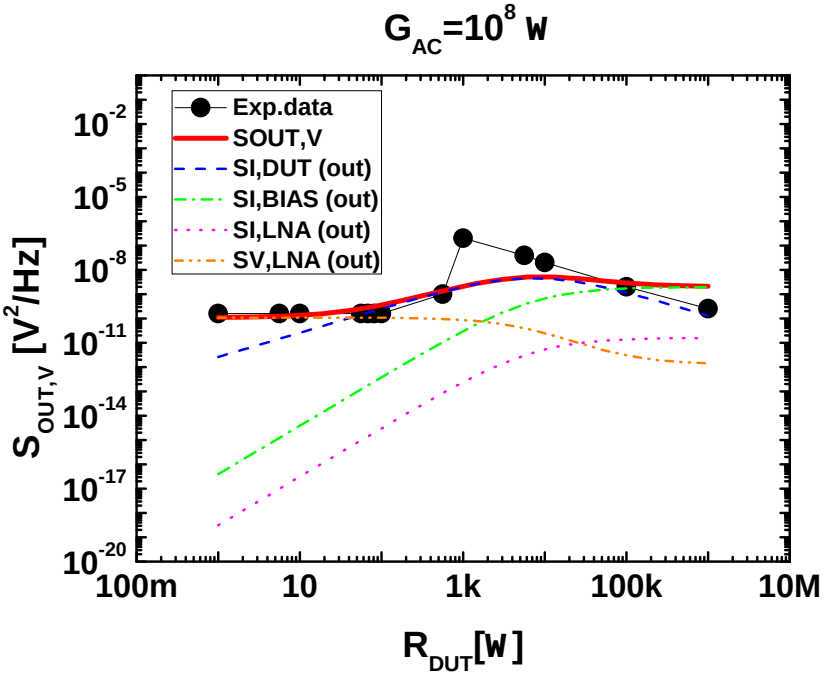


Figure 3.23: Lines: $S_{OUT,V}$, $S_{I,DUT}(out)$, $S_{I,BIAS}(out)$, $S_{I,LNA}(out)$ and $S_{V,LNA}(out)$ as a function of R_{DUT}, calculated using Eq.(3.33) and Eq.(3.35), for $G_{AC} = 10^8\Omega$. Dots refer to experimental $S_{OUT,V}$ data.

calculated using Eq.(3.37), we obtain the current noise PSD magnitudes shown in Figure 3.28 as a function of I_D, and displayed in Figure 3.29 as a function of frequency f for different I_D. For the calculations, R_{DUT} is imposed equal to the dynamic resistance of the diode r_d given by:

$$r_d = \frac{\partial V_D}{\partial I_D}, \tag{3.38}$$

where V_D is the applied voltage, related to I_D by:

$$I_D = I_0 \exp\left(\frac{\eta V_D}{V_{TH}}\right). \tag{3.39}$$

I_0 is derived by fitting, in our device η=1.87, and $V_{TH} = 26$ mV is the thermal voltage. The current noise PSD is measured using $G_{AC} = 10^6\Omega$, since in the chosen I_D range (10 μA $\leq I_D \leq$ 108 μA), we have $445\Omega \leq R_{DUT} \leq 4.8\text{k}\Omega$, that belongs to the region where Eq.(3.33) fits the experimental system response. As shown in Figure 3.28 and in Figure 3.29 the agreement between measurements and model is very good, suggesting once again that our analytical model is able to extract the DUT noise contribution from all the other noise sources.

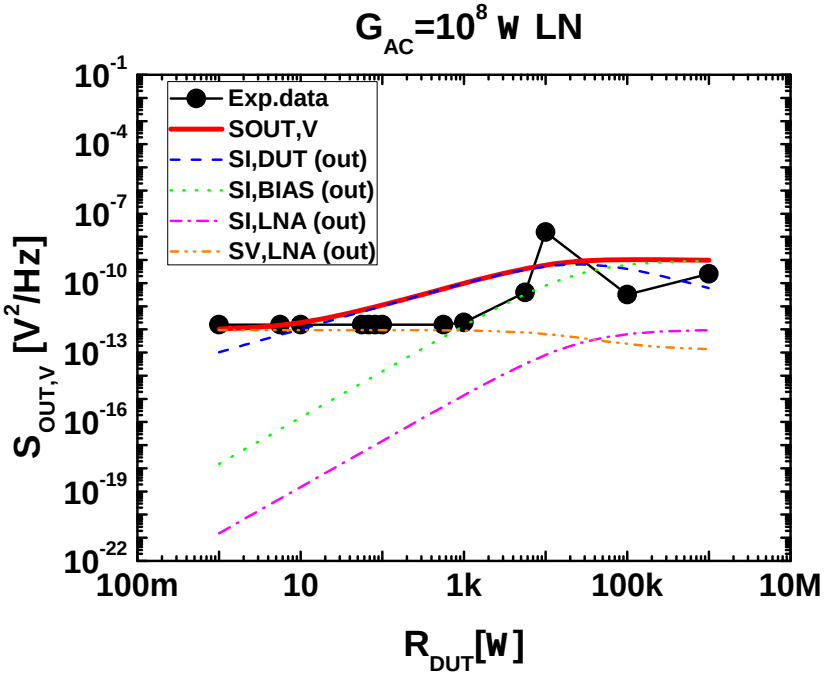


Figure 3.24: Lines: $S_{OUT,V}$, $S_{I,DUT}(out)$, $S_{I,BIAS}(out)$, $S_{I,LNA}(out)$ and $S_{V,LNA}(out)$ as a function of R_{DUT}, calculated using Eq.(3.33) and Eq.(3.35), for $G_{AC} = 10^8\Omega$ low-noise. Dots refer to experimental $S_{OUT,V}$ data.

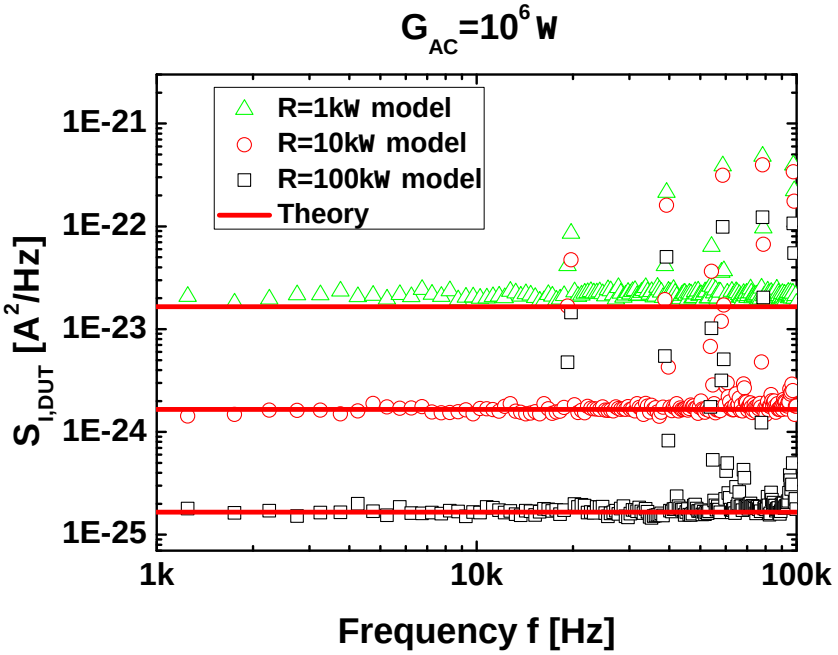


Figure 3.25: $S_{I,DUT}$ as a function of frequency f, model -Eq.(3.34)- (dots) vs. theoretical values -Eq.(3.36)- (solid lines), for 1kΩ, 10kΩ and 100kΩ resistances with $G_{AC} = 10^6\Omega$.

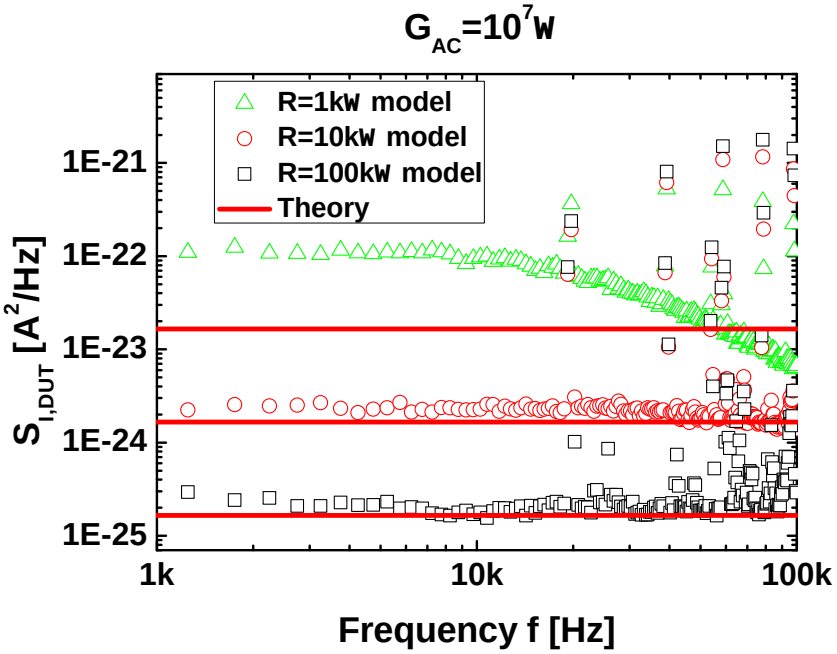


Figure 3.26: $S_{I,DUT}$ as a function of frequency f, model -Eq.(3.34)- (dots) vs. theoretical values -Eq.(3.36)- (solid lines), for 1kΩ, 10kΩ and 100kΩ resistances with $G_{AC} = 10^6\Omega$.

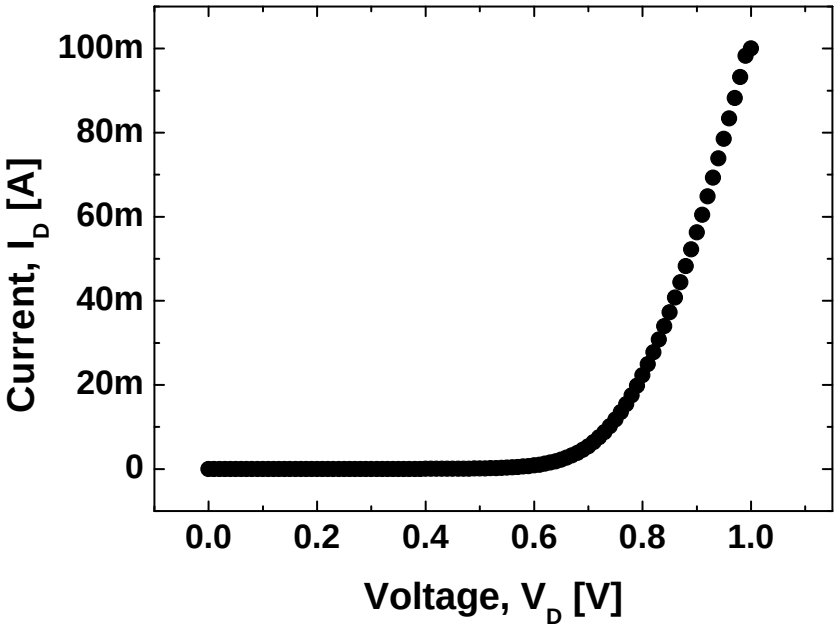


Figure 3.27: $I_D - V_D$ characteristics of the diode under test (direct polarization).

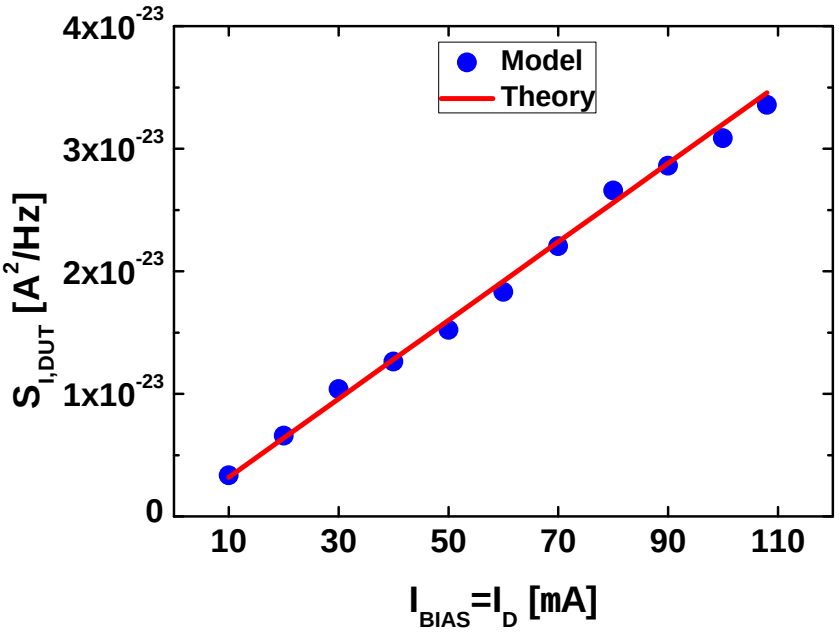


Figure 3.28: $S_{OUT,V}$ of the diode under test as a function of $I_{BIAS} = I_D$: experimental data (dots) and model (solid line). $G_{AC} = 10^6\Omega$.

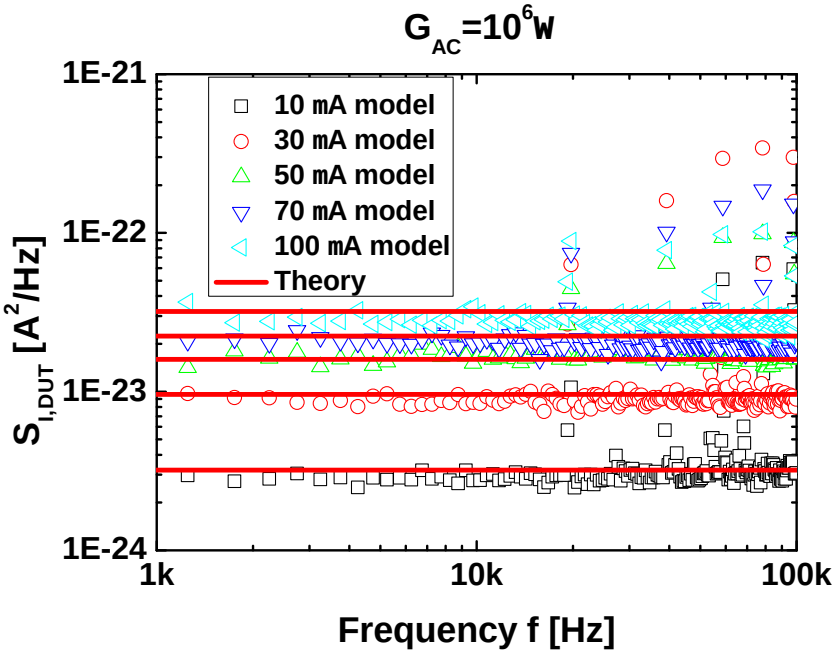


Figure 3.29: $S_{OUT,V}$ of the diode under test as a function of frequency f, for different values of $I_{BIAS} = I_D$ (see legend): experimental data (dots) and model (solid line). G_{AC} is set to $10^6\Omega$.

3.11 Application: low-frequency noise in polycrystalline Phase-Change Memory

As an example of application of the noise setup we measure the low-frequency noise of polycrystalline Phase-Change Memory (PCM) devices, recently assessed in literature [Fan08]. Our test devices, the same of [Fan08], have been fabricated by Numonyx [Pel04]. $I-V$ characteristics and corresponding R_{DUT} are displayed in Figure 3.30. It is clear that R_{DUT} is approximately a constant of value ~ 5.7 kΩ. So, employing an AC gain $G_{AC} = 10^6\Omega$ we fall in the well fitted region of Figure 3.21. In Figure 3.31, we show the current noise PSD of a reference PCM device varying the polarization current I_{BIAS}. Our spectra show a $1/f^{1.1}$-like behavior, and a current noise PSD that significantly increases with I_{BIAS}, in accordance with the previous literature on the subject [Fan08]. In this case, the setup-induced noise contribution and the non-ideality of the instrumentation are negligible. To demonstrate this statement consider Eq.(3.34). The equipment contribution gives a whole S_I expressed by (refer to Table 3.2 for noise and R_{IN} parameters at $G_{AC} = 10^6\Omega$):

$$S_{I,BIAS} + S_{I,LNA} + \frac{S_{V,LNA}}{\left(R_{DUT}||R_{BIAS}\right)^2} \sim 1.28 \cdot 10^{-24}, \tag{3.40}$$

well below the $S_{I,DUT}$ order of magnitudes shown in Figure 3.31. Moreover, the term:

$$\left[\frac{(R_{DUT}||R_{BIAS}) + R_{IN}}{R_{DUT}||R_{BIAS}}\right]^2 \sim 1.0038, \tag{3.41}$$

and so, in this case, due to the intrinsic high noise level of the polycrystalline PCM, we can effectively compute $S_{I,DUT}$ as the setup would be ideal, that is by simply calculating:

$$S_{I,DUT} = \frac{S_{V,OUT}}{{G_{AC}}^2}. \tag{3.42}$$

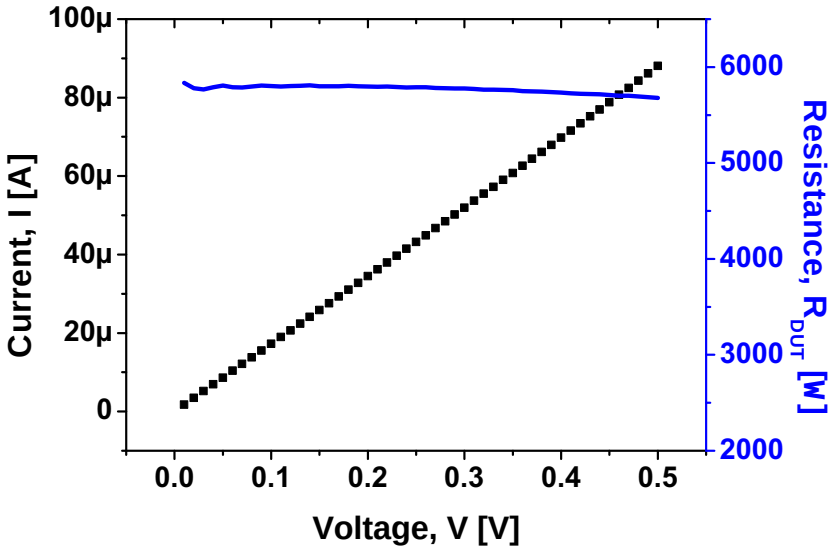


Figure 3.30: $I - V$ characteristics (dots) and resistance $R_{DUT} = V/I$ (solid line) of the PCM device under test.

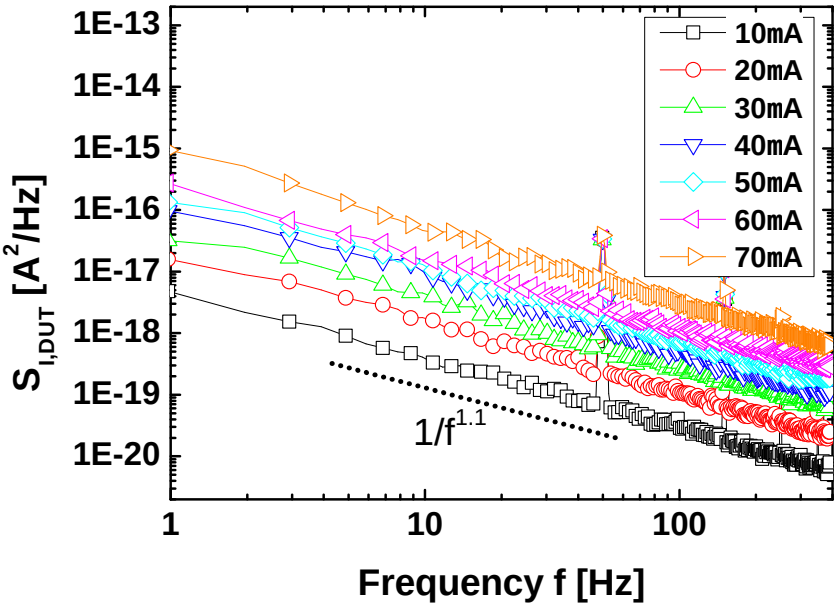


Figure 3.31: $S_{I,DUT}$ of the PCM device under test as a function of frequency f for different values of I_{BIAS} (indicated in the legend).

3.12 Conclusions

An experimental setup for low-frequency noise measurements on two-terminal solid-state devices has been successfully implemented. An analytical formula -Eq.(3.34)- allowing to calculate the current noise PSD of the DUT, $S_{I,DUT}$ by subtracting the

measurement system induced intrinsic noise has been derived. Our measurement equipment is able to reproduce noise data on resistors, diodes and Phase-Change Memory in accordance with theory and recent literature.
Moreover, the analysis of the noise contribution induced by the LNA has pointed out that for each AC gain G_{AC} there is only a specific interval of measurable *allowed* R_{DUT} values; measuring in the *not-allowed* range can lead to errors (e.g. spectrum cut-off, see Figure 3.26) due to the physical limitation (resonance phenomena) of the LNA. In particular, R_{DUT} in the range $10\ \Omega < R_{DUT} < 70\ \Omega$ cannot be measured with enough reliability by using the LNA *EG&G 5182*

3.13 Acknowledgments

The author gratefully acknowledges the expertise of Professor Mattia Borgarino of *Università degli Studi di Modena e Reggio Emilia* for his fundamental contribution to this project, from the realization of the current bias circuit, through connector choices, to the use of the Dynamic Signal Analyzer, the review process and many others. Many thanks also to Valerio Doga for the experimental measurements and to Roberto Formentini for the fabrication of the connection interfaces.

Chapter 4

Assessment of self-induced Joule-heating effect in the $I - V$ readout region of polycrystalline $Ge_2Sb_2Te_5$ Phase-Change Memory

4.1 Abstract

The physical mechanisms which regulate carrier transport in polycrystalline chalcogenides, such as $Ge_2Sb_2Te_5$ (GST), are still debated. Recently, Self-induced Joule-Heating (SJH) effect has been claimed to be the key factor to explain the non-linearity of the $I - V$ characteristics of polycrystalline GST-based Phase-Change Memory (PCM). In this Chapter, we carefully investigate the SJH occurring in the GST material by analyzing the $I - V$ characteristics of PCM cells at low voltages, i.e. in the memory cell readout region. To accomplish the study, we use ad-hoc fabricated PCM devices allowing an easier evaluation of SJH occurring in the chalcogenide layer. A novel procedure to test the SJH effect is also proposed. Comparison between numerical simulations and compact modeling is discussed as well. Our work shows that SJH effect is not sufficient to reproduce the experimental $I - V$ non-linearity, claiming for new experiments and theoretical investigations. Therefore, this work can be considered a step forwards towards the comprehension of the transport properties of polycrystalline GST, which is a key aspect for robust modeling of PCM devices.

4.2 Introduction

Phase-Change Memory (PCM) is considered among the most promising next-generation non-volatile memory technologies. PCM has potential of outstanding scalability (down to few nanometers), very fast programming (in the range of nanoseconds) and high endurance (up to 10^9 cycles) [Bez09]−[Ser09]. The PCM device is basically a programmable resistor made of a thin layer of a chalcogenide alloy sandwiched between an electrode contact and a heater plug. By applying suitable electrical pulses to the device, the PCM cell can switch between two states: the amorphous high-resistance state (named RESET) and the polycrystalline low-resistance one (SET). The most used and known chalcogenide material is an alloy made by germanium, antimony and tellurium: $Ge_2Sb_2Te_5$, named GST.

Recently, analytical modeling of charge transport in GST amorphous phase has been thoroughly addressed in literature, concerning both $I-V$ characteristics [Iel06]−[Red08] and low-frequency noise [Fan06]−[Fug10b]. On the other hand, modeling of the transport properties of polycrystalline GST has not been covered in such details. Nevertheless, the understanding of the $I-V$ behavior in the readout region of the polycrystalline memory cells is very important, especially for multilevel PCM technology, where the capability to discriminate between close SET current levels is crucial [Nir07]. Up to today, two models addressing the $I-V$ behavior of SET state PCM have been presented in literature. In the following, we briefly discuss these models.

Pirovano et al. proposed a classical semiconductor physics approach based on Poisson's law, drift-diffusion equations, Shockley-Hall-Read recombination-generation, and heat conduction [Pir04][Fer10]. The band gap of polycrystalline face-centered cubic (*fcc*) GST is investigated and the presence of structural vacancies in the GST lattice is modeled by introducing traps in the energy gap. However, neither accordance between model and $I-V$ data as a function of temperature is examined, nor the temperature dependence of the many model fitting parameters (e.g. density of states, energy of traps, and mobility) is disclosed. Moreover, the importance of the role played by Joule-heating, accounted in the model by means of the heat transport equation, is not discussed.

On the other hand, *Ventrice et al.* reproduce the experimental $I-V$ characteristics using a compact modeling approach, based on Ohm's law and Joule-heating [Ven07]. The model consists of a compact electro-thermal circuit of the memory cell, in which Joule-heating occurring in the chalcogenide material is claimed to be the key parameter to justify the experimental non-linearity of the $I-V$ curve [Ven09]. This model considers indeed polycrystalline GST as a simple resistor, which electrical conductivity

depends only on temperature, hence neglecting its possible field-driven dependence.
In this framework, our work aims to rigorously investigate the effect of Joule heating in the readout region of polycrystalline GST-based PCM devices, by means of $I-V$ experimental characterization at different temperatures and electro-thermal simulations. In particular, our goal is to check, using a multi-physics simulation approach, if a simple ohmic model is really capable of reproducing the $I-V$ experimental behavior.
In our study, we use ad-hoc fabricated lance-type PCM test cells. In our devices, the heater is a wide W plug, which electrical and thermal resistances are low compared to the GST ones. For this reason, the analysis of our device allows a much simpler evaluation of the SJH effect occurring in the GST layer compared to other memory technologies using resistive narrow heaters [Pel04][Pir08], to which are applied the above models. In fact, due to the material and geometrical properties of the heater in our devices, the temperature rise during cell operation occurs only in the GST layer [Bra11], rather then at the heater-GST interface like in [Pir04][Red08][Fer10][Ven07][Ven09], where SJH modeling is more complicated, since it should require also an accurate a-priori characterization of the temperature dependence of the heater electrical and thermal resistivities.
The manuscript is organized as follows. Section 4.3 reports a brief description of the PCM devices under test and the $I-V$ characterization as a function of temperature. Section 4.4 qualitatively discusses the physics of the SJH effect. In Section 4.5, the electro-thermal model implemented in this work is described in detail. Section 4.6 shows the results of the $I-V$ simulations. Section 4.7 proposes a novel method to test the SJH effect to corroborate the results of the $I-V$ simulations. In Section 4.8, we compare the findings obtained by numerical simulations with a classical compact modeling approach. Then, Section 4.9 briefly discuss possible future perspectives of polycrystalline GST carrier transport modeling. Finally, Section 4.10 draws the conclusions of our study.

4.3 Experimental characterization

4.3.1 PCM test devices

Devices used in this work are lance-type PCM cells where a 100nm-thick phase-change layer is deposited on the top of a 300nm-wide, and 300nm-thick, cylindrical W plug. Cu and Al are used as top and bottom electrodes, respectively (see Figure 4.1).
In the fabrication process, the GST material has been deposited at room temperature,

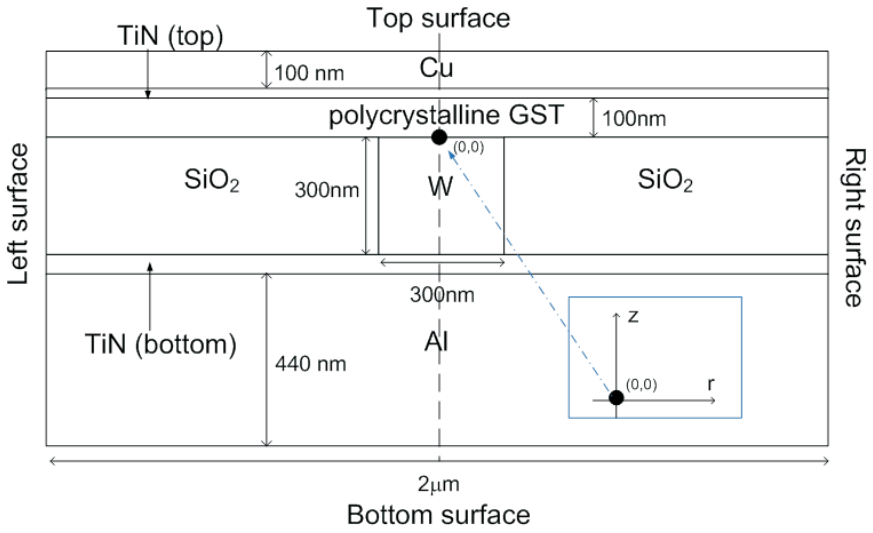


Figure 4.1: Schematic of the cross section of our lance-type PCM device (to scale). The core of the memory cell is a 100-nm thick polycrystalline GST layer, placed on a 300-nm wide and 300-nm thick cylindrical W plug, and insulating material, SiO_2. Top and bottom electrodes are made of Cu and Al, respectively. The two TiN thin depositions (TiN (top) thickness=25nm, TiN (bottom) thickness=50nm) act as adhesion layers and diffusion barriers. The (0,0) point (black dot), origin of our 2D reference system of polar coordinates r-z indicated in the figure inset, is set at the interface between GST and W, along the vertical axis of symmetry of the device (vertical dash-type line).

i.e. in the amorphous state. In the manufacturing flow, 200°C has been the maximum thermal budget. Then, at fab-out, the PCM devices have been crystallized by thermal annealing at 200°C for 15 minutes. After this treatment, the GST structure is (polycrystalline) fcc [Lom09]. Note that the polycrystalline GST can exist in two possible lattice configurations: the stable hexagonal hcp structure and the meta-stable face centered cubic fcc lattice [Yam91]. However, since the metastable phase crystallizes faster [Yam91], in real memory array operations, the polycrystalline GST is always in the fcc phase. For this reason, the study of the $I-V$ behavior of fcc GST is of primary importance.

4.3.2 $I-V$ characteristics as a function of temperature

Figure 4.2 shows the $I-V$ characteristics of our PCM devices at different ambient temperatures T_{amb} =25°C, 45°C, 65°C, and 85°C. Four-probes $I-V$ measurements are performed using a HP4155 parameter analyzer equipped with a thermochuck system.

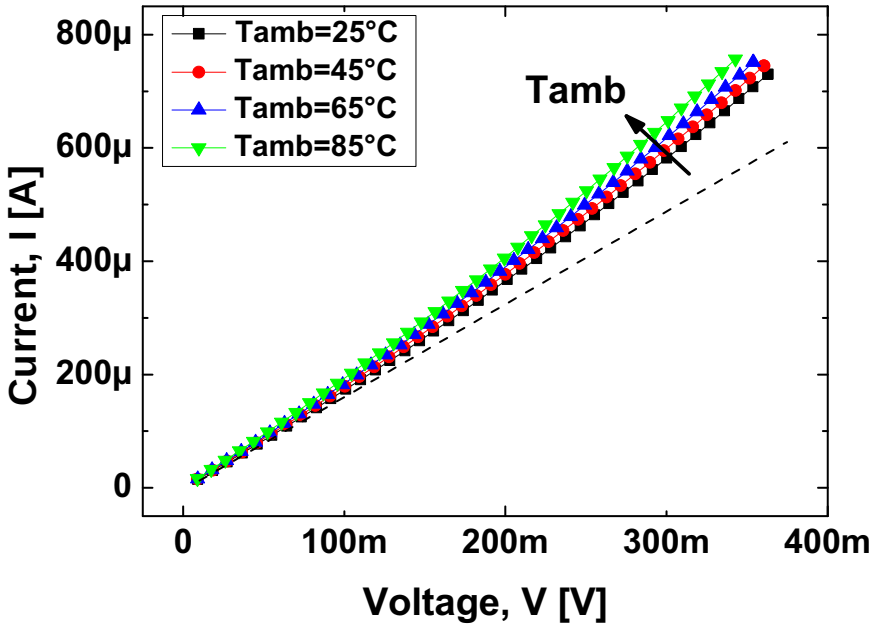


Figure 4.2: Experimental $I-V$ characteristics at low voltages (i.e. readout region) of our fcc GST-based PCM cells at T_{amb} =25°C, 45°C, 65°C, and 85°C (symbols+line plots). In dash-type line the linear extrapolation of the ohmic region of the curve at T_{amb} =25°C.

The voltage V is imposed to the cell, while the current I is read. We measured the $I-V$ curve at low voltages in order to investigate the cell current in the PCM readout region.
Interestingly, the $I-V$ characteristics exhibits a strict ohmic behavior only at very low voltages (i.e. $V \leq 100$ mV). At higher voltages, the $I-V$ characteristics progressively deviates from a pure resistive line, showing a non-linear increase of the current. Furthermore, as well known [Lom09]−[Lye06], the fcc GST electrical conductivity increases with temperature.

4.4 The Self-induced Joule-Heating effect (SJH)

From a qualitative point of view, the phenomenology of the SJH effect occurring in the GST layer can be understood by considering the following basic physical reasons. When a voltage is imposed across the electrodes of the PCM device, a correspondent electric field (**E**) distributes according to the electrical conductivity (σ) of the different layers,

originating a current density $\mathbf{J} = \sigma\mathbf{E}$. Since in our device the electrical conductivity of GST is much lower (more than 2 orders) compared to those of the other materials in the stack, the electric field, as well as the current density flow, concentrate within the GST material, and at the GST-W interface. Current crowding increases the temperature in the chalcogenide due to Joule power generation $\mathbf{J} \cdot \mathbf{E}$. The increase of temperature T induces an increase of GST electrical conductivity, that leads to an augmentation of the current density, which, in turn, will further rise T. This positive-feedback process is counterbalanced by heat flux from the GST layer to the metal electrodes, which is proportional to heat generation and is limited by GST thermal conductivity ($k_{th,GST}$). Steady-state is reached once heat flux and the generated electro-thermal power balance one another.

Note that $k_{th,GST}$ is, at room temperature, in the 0.28-0.55 [W/(K·m)] range [Fal09]−[Gir05], being more than three orders lower compared to those of metal electrodes and heater. For this reason, the GST layer represents the bottleneck for heat dissipation in the device, concentrating the heating effects (i.e. the temperature gradient) in the active layer of the memory cell. Nevertheless, it is worth noticing that $k_{th,GST}$ increases with temperature [Fal09]−[Gir05], leading to a more efficient heat dissipation in the device, and so alleviating the positive feedback phenomenon triggered by Joule-heating.

According to this physical picture, in the linear $I-V$ region the temperature increase due to SJH is negligible, and the polycrystalline material shows an ohmic behavior. On the other hand, at higher voltages, the temperature inside the phase-change material rises due to SJH, boosting the GST electrical conductivity and yielding the non-linear current increase observed in Figure 4.2. In this framework, since the electric field effects on σ are assumed to **be** negligible, this phenomenon has been described in [Ven09] as "apparent deviation from Ohm's law".

In order to quantitatively analyze the SJH effect in our PCM devices, we simulate the coupled electro-thermal model described in the next Section.

4.5 Electro-thermal model

The electro-thermal model implemented consists of two coupled partial differential equation (PDE) modules [Rus08][Bra08]: (1) a DC electrical conduction module, with V as dependent variable, and (2) a steady-state heat conduction module, which solves for T. The two PDE modules are coupled by means of the T-dependence of the GST electrical conductivity and the Joule power dissipated. The main goal of the model is to simulate the $I-V$ characteristics of the PCM device.

It is worth noticing that each point of the $I-V$ can be considered a steady-state working point. This is because the $I-V$ measurement consists in a staircase-up voltage pulse chain in which the time duration of each pulse is in the order of tenths of μs, that is much higher than the time required to our PCM device to reach a steady-state condition temperature distribution, which is about 100 ns [1].
In the following, the two PDE modules are described in detail.

4.5.1 Mesh parameters in 2D-axial symmetry

The electro-thermal model has been solved by using FEM numerical methods. Because of the cylindrical symmetry of the device, the simulations have been performed using a 2D-axial symmetry system of coordinates. The grid comprises 21645 nodes and 42976 elements, and is heavily refined especially at the heater-GST interface.

4.5.2 DC electrical conduction

The DC electrical conduction module solves for:

$$-\nabla \cdot (\sigma \nabla V) = 0. \tag{4.1}$$

Eq.(4.1) combines the continuity equation, Ohm's law and the definition of electric potential, respectively:

$$\begin{cases} \nabla \cdot \mathbf{J} = 0, & (4.2) \\ \mathbf{J} = \sigma \mathbf{E}, & (4.3) \\ \mathbf{E} = -\nabla V. & (4.4) \end{cases}$$

In order to investigate if a pure ohmic model could be applied to polycrystalline GST, our simulator treats the chalcogenide material like a metal by implementing Laplace's equation instead of Poisson's equation, assuming no space-charge region in the GST domain. The boundary conditions set to V are specified in Table 4.1, in which boundary labels refer to Figure 4.1, and $\hat{n}$ is a outward unit vector with direction perpendicular to the reference surface. As initial condition on V, we considered a linear drop of the voltage potential from the top electrode towards bottom electrode. The model of the GST electrical conductivity is described in the next paragraph, while, the σ of the other materials in the stack are listed in the second column of Table 4.2 (ref. to [CRC]).

[1] This time duration has been calculated by means of transient heat transport simulations by solving the transient Fourier's heat conduction postulate, with specific heat and density parameters taken from literature [CRC][Kan03]

Boundary	Condition
Top surface	fixed V potential
Left/Right surfaces	$\hat{n} \cdot \mathbf{J} = 0$ (electrical insulation)
Bottom surface	$V = 0$ (ground)

Table 4.1: Boundary conditions for DC electrical conduction.

4.5.3 GST conductivity model

The T-dependence of polycrystalline GST electrical conductivity is implemented through the Arrhenius law [Ven09][Kat05]:

$$\sigma = \sigma_0 \exp\left(\frac{-E_A}{K_B T}\right), \tag{4.5}$$

where E_A is the activation energy and K_B is the Boltzmann constant.

- E_A= 14.1 meV is extracted by fitting of experimental electrical conductance $G = I/V$ as a function of $1/(K_B \cdot T)$, according to:

  $$G = G_0 \exp\left(\frac{-E_A}{K_B T}\right). \tag{4.6}$$

  As shown in Figure 4.3, the agreement between data and model is very good.
  It is worth noticing that, for each T, G has been calculated at $V = 10$ mV, since at very low V the electro-thermal coupling is negligible (linear $I-V$). For this reason, in Eq.(4.6), the actual temperatures of the GST layer are set equal to T_{amb}.

- To determine σ_0 avoiding geometrical approximations (e.g. cylindrical/conical conduction hypothesis that should be necessary to analytically calculate σ_0 from G_0), we simulate the DC electrical conduction module at very low V (i.e. no electro-thermal coupling), and find σ_0 by successive approximations. Very good fitting is obtained using σ_0=1.386·10^3 $(\Omega\cdot\text{m})^{-1}$.

4.5.4 Steady-state heat conduction module

The steady-state heat conduction module solves for the following equation,

$$-\nabla \cdot (\kappa_{th} \nabla T) = \sigma \nabla V^2, \tag{4.7}$$

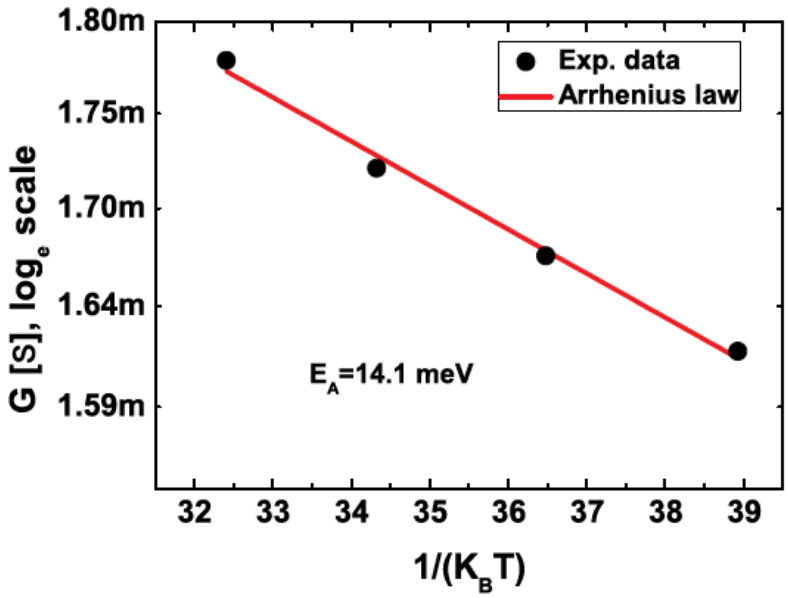


Figure 4.3: G ($\log_e$-scale) as a function of $1/(K_B \cdot T)$, where $T_{amb} = 25°C$, 45°C, 65°C, and 85°C. Dots are experimental data, solid line is fitting by using Eq.(4.6). Activation energy E_A = 14.1 meV.

Material	σ [$(\Omega \cdot$ m$)^{-1}$]	κ_{th} [W/(K·m)]
Cu	$5 \cdot 10^7$	400
TiN	$1.2 \cdot 10^6$	19.2
W	$8.6 \cdot 10^6$	170
SiO_2	$1 \cdot 10^{-14}$	0.7
Al	$3.6 \cdot 10^7$	240

Table 4.2: Electrical conductivity (σ) and thermal conductivity (κ_{th}) parameters used in this work (GST parameters are discussed apart in the text).

Boundary	Condition
Top surface	T_{amb}
Left/Right surfaces	$\hat{n} \cdot (\kappa_{th} \nabla T) = 0$ (thermal insulation)
Bottom surface	T_{amb}

Table 4.3: Boundary conditions for steady-state heat conduction.

which combines the steady-state Fourier's heat conduction postulate and the Joule equation (i.e. electro-thermal power), respectively given by:

$$\begin{cases} -\nabla \cdot (\kappa_{th} \nabla T) = Q, & (4.8) \\ Q = \mathbf{E} \cdot \mathbf{J} = \sigma \nabla V^2. & (4.9) \end{cases}$$

The boundary conditions of this problem are specified in Table 4.3. The initial condition on the temperature is $T = T_{amb}$ in the whole domain. Importantly, thermal conductivity of polycrystalline GST has been previously measured on our test devices by means of the *3ω method* [Cah94]. These test structures have previously been annealed at the same conditions applied for the devices used for $I-V$ simulations. At room temperature we measured $\kappa_{th,GST} \sim 0.3$ W/(m·K), which fits in the interval of GST thermal conductivity values reported in literature [Fal09]−[Gir05]. Given the restricted T range investigated (25°C$\leq T \leq$ 85°C), this value is considered T-independent. Note that, since $\kappa_{th,GST}$ increases with increasing T [Fal09][Lye06], neglecting its T-dependence leads to a slight overestimation of the SJH effect. The κ_{th} values used in the simulations for the other materials in the stack are listed in the third column of Table 4.2 (ref. to [CRC]).

4.5.5 Thermal boundary resistances

Due to difficulty of getting experimental characterization data on interfacial properties of our devices, we neglect the possible presence of significative thermal boundary resistances at the TiN-GST and GST-W interfaces. Thermal boundary resistance (TBR) [K·m^2/W] are reported to have a not-negligible role on programming operation [Fer10][Rei08], since melt GST shows a very low electrical resistance. However, TBRs effect is expected to be less important in the cell readout region, because, in this case, GST is much more resistive. Moreover, since our device has a very large GST-W

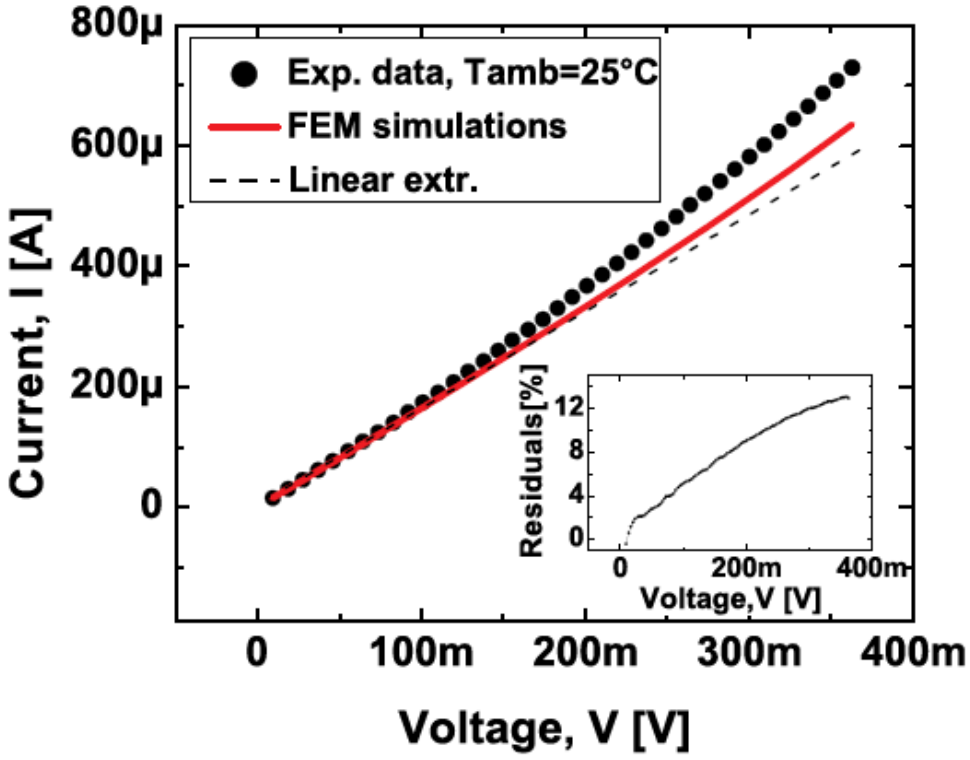


Figure 4.4: Electro-thermal FEM simulations of $I-V$ curve with T_{amb} =25°C (solid line) and experimental data at the same temperature (dots). Dash-type line is the extrapolation of the linear region of the experimental curve. In the inset we plot fit residuals (in %) as a function of V.

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contact area, the overall thermal resistances (=TBR/area, [K/W]) of the very thin interfacial layers (few nm) are expected to be sensibly lower compared to the GST one. The same qualitative considerations hold also for electrical boundary resistances, which are frequently assumed to be derived from the Wiedemann-Franz relation, which states that thermal and electrical resistivities are proportional [Ash76]. For SJH investigation purposes, these reasonable assumptions are indeed other benefits which come from our relaxed device architecture.

4.6 $I-V$ simulations

In Figure 4.4, the $I-V$ characteristics obtained from simulations is shown against experimental data (T_{amb} =25°C). The figure also shows the linear extrapolation of the $I-V$ curve at low V (dash-type line). As it appears clear, the simulated current, (I_{sim}),

whereas sensibly distinguishing from the pure linear behavior, does not well reproduce the experimental current (I_{exp}), underestimating the slope of the $I-V$ non-linearity. In fact, as shown in the figure inset, fit residuals (i.e., $(I_{exp}-I_{sim})/I_{exp}\cdot 100$) increase with increasing V. Remarkably, for the highest measured $V\sim 0.36$ V, the SJH model leads to an error in the predicted current in the order of 12%. The same conclusion holds also for the other T_{amb}.

To further investigate, we have performed simulations by decreasing $\kappa_{th,GST}$ in order to identify which GST thermal conductivity would have allowed reproducing the $I-V$ characteristics. The best fit is obtained by using $\kappa_{th,GST}=0.11$ W/(K·m). However, we note that fitting quality is not perfect, since the slope of $I-V$ curve at the different voltage regions is not well reproduced. Then, more importantly, note that to get a reasonable fit of experimental data we must use thermal conductivity values much lower than the characterized 0.3 W/(m·K), and also far from the measurements reported in literature, ranging from 0.28 to 0.55 W/(K·m) [Fal09]−[Gir05]. Moreover, considered indeed that thermal conductivity of *amorphous* GST has been measured to be about 0.20 W/(m·K) [Fal09]−[Gir05]. For these reasons, the $\kappa_{th,GST}$=0.11 W/(K·m) used in the fitting, even lower than the one of amorphous GST, has poor physical sound.

To conclude the analysis of the simulated $I-V$, we argue that the SJH ohmic model does not well reproduce the experimental data, suggesting that the increase of GST electrical conductivity by field effect is indeed not negligible.

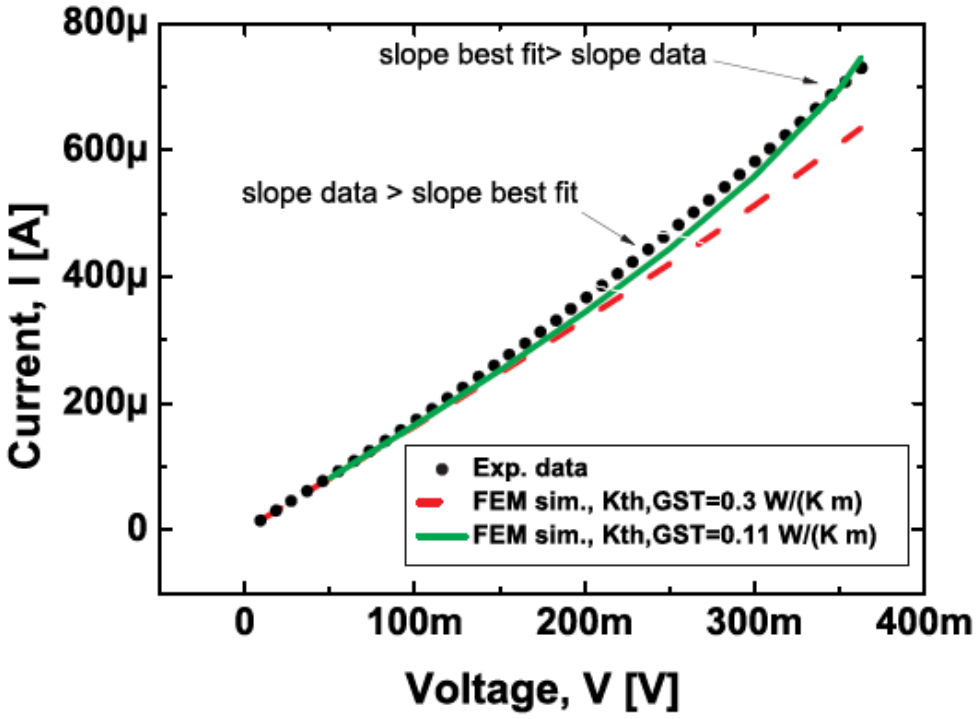

Figure 4.5: Electro-thermal FEM simulations of $I - V$ curve with $\kappa_{th,GST}$=0.3 W/(m·K) (dash line, red), $\kappa_{th,GST}$=0.11 W/(m·K) (solid line, green), and experimental data (dots). Both data and simulations refer to T_{amb}=25°C. The best fit curve ($\kappa_{th,GST}$=0.11 W/(m·K) at "medium" V range ($150mV < V < 300mV$) underestimates the slope of experimental data. The opposite happens at $V > 350mV$, where model increases quicker than data.

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4.7 A novel procedure to evaluate SJH: test of necessary condition

To analyze more in depth the results of the simulations, we introduce a novel test procedure.

We consider two of the experimental $I-V$ curves (for example, the one at T =25°C and the one at T =85°C). We plot, in the same graph (see Figure 4.6), (i) the experimental $I-V$ curve referring to the lower temperature (in this case to T =25°C); and (ii) the *extrapolation of the linear region* of the other $I-V$ curve at the higher T (in this example, we extrapolate the linear part of the $I-V$ at T =85°C). Then, we check for the voltage value V^* at the intersection between the two curves. V^* is determined by a numerical routine which finds for the voltage value to which corresponds the minimum distance (in *abs*) between the two curves (in this example V^* =183.2 mV). Note that, *for the experimental $I-V$ non-linearity to be ascribed to SJH effect*, at $V=V^*$, the maximum temperature inside the PCM device, T_{max}, must be *higher* then the ambient temperature referring to the linearly-extrapolated curve (in this example, it must have been T_{max} >85°C). The fulfillment of this inequality can be considered a *necessary condition* for SJH to be the only mechanism responsible for the $I-V$ non-linearity. In fact, since GST conductivity increases with T, for the temperature distribution in the PCM device heated up from 25°C to have the same effect on current that a constant T_{amb} =85°C in the whole device, at least one point in the system must have T higher than 85°C.

To show the results of the application of the above method, we plot, in Figure 4.7, T as a function of the radial coordinate r on a cut line corresponding to $z=50$ nm (vertical center of GST layer) [2]. The maximum simulated temperature in the device is $T\sim$ 45°C, well below 85°C. This evidence confirms the findings of the $I-V$ simulations shown in Figure 4.4, suggesting once again that the contribution of SJH is not sufficient to explain the $I-V$ experimental non-linearity. The same qualitatively conclusions can be drawn considering the other "temperature couples", for which the results of the simulations are summarized in Table 4.4.

[2]FEM simulations to which refers this Section have been carried out using the measured $\kappa_{th,GST}$ =0.3 W/(m·K), coherently with $I-V$ simulations of Figure 4.4.

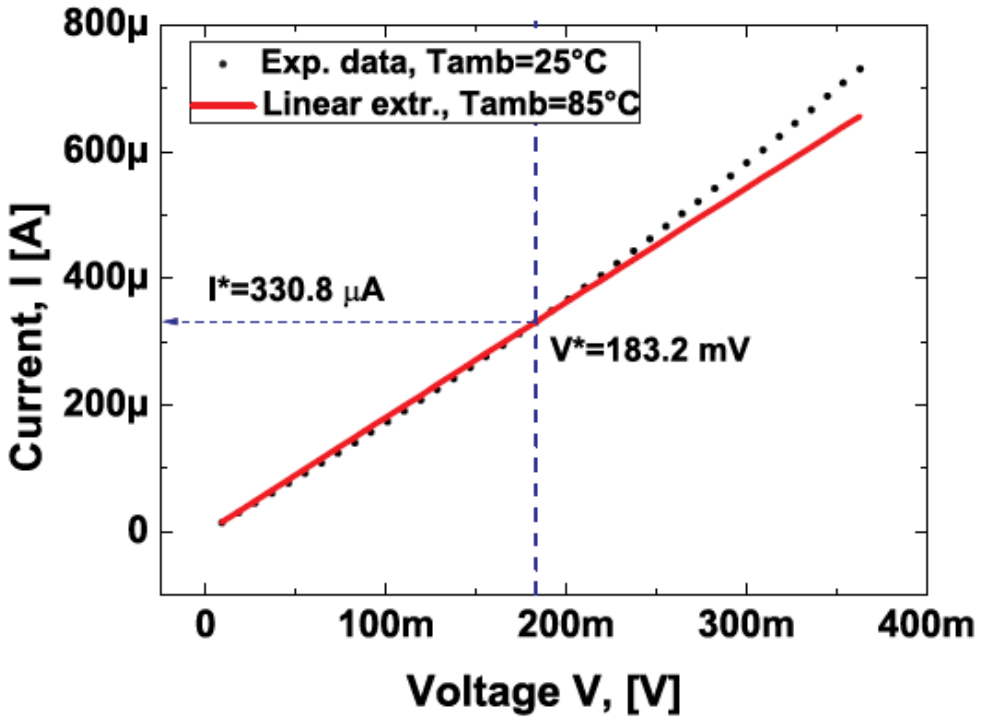

Figure 4.6: Experimental $I-V$ curve at 25°C (dots) and linear extrapolation of $I-V$ curve at 85°C (solid line). The intersection between the two curves occurs at $V = V^*$.

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T couples	simulated T_{max}
25°C and 45°C	35°C
45°C and 65°C	52°C
65°C and 85°C	71°C

Table 4.4: T couples and simulated T_{max} referring to the test procedure explained in Section 4.7.

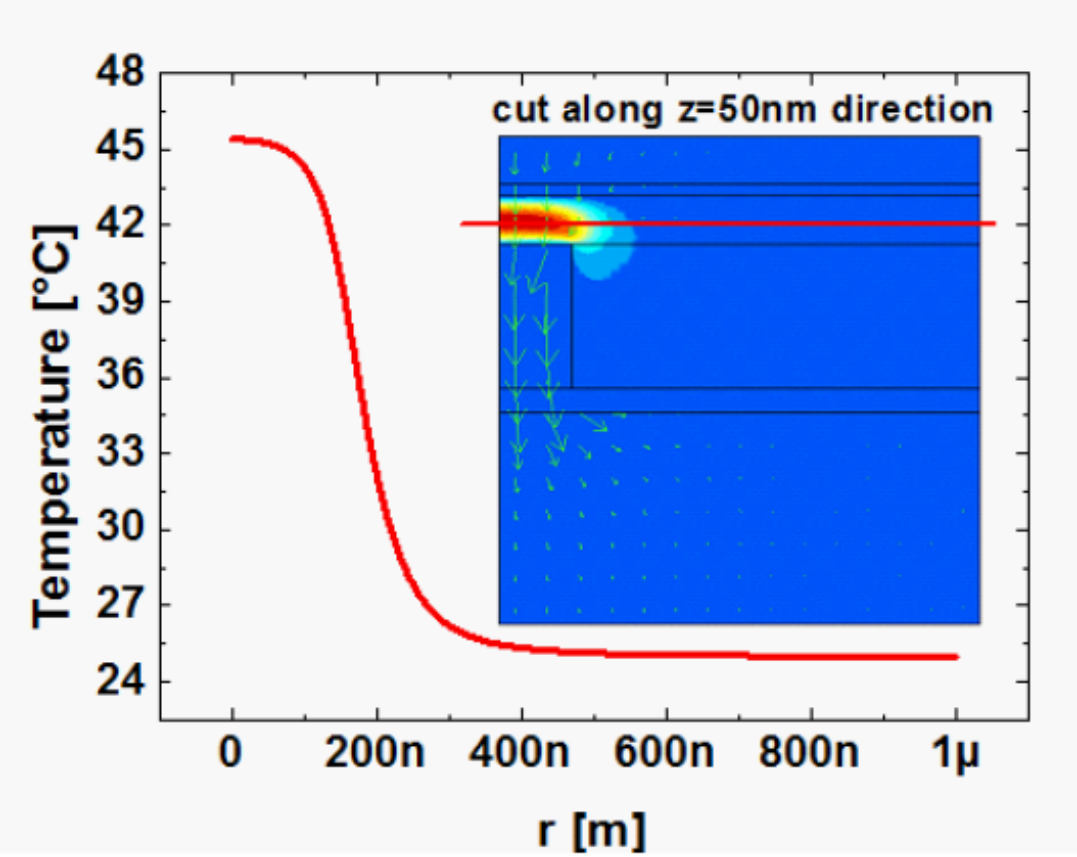

Figure 4.7: Simulations of temperature (2D axial-symmetry) as a function of r for a cut along the $z = 50$nm direction (horizontal line), i.e. at the vertical center of the GST layer, $T_{max} \sim 45$°C, T_{amb} =25°C. As indicated by the temperature color map in the figure, in our cell all the heating effects (i.e. temperature rise from T_{amb}) are concentrated inside the GST region. In fact, electrodes and heater plug, that are very efficient heat and current sinks compared to GST, remain at $T = T_{amb}$ [Bra11]. In the simulations, the applied voltage V is equal to the V^* =183.2 mV shown in Figure 4.6.

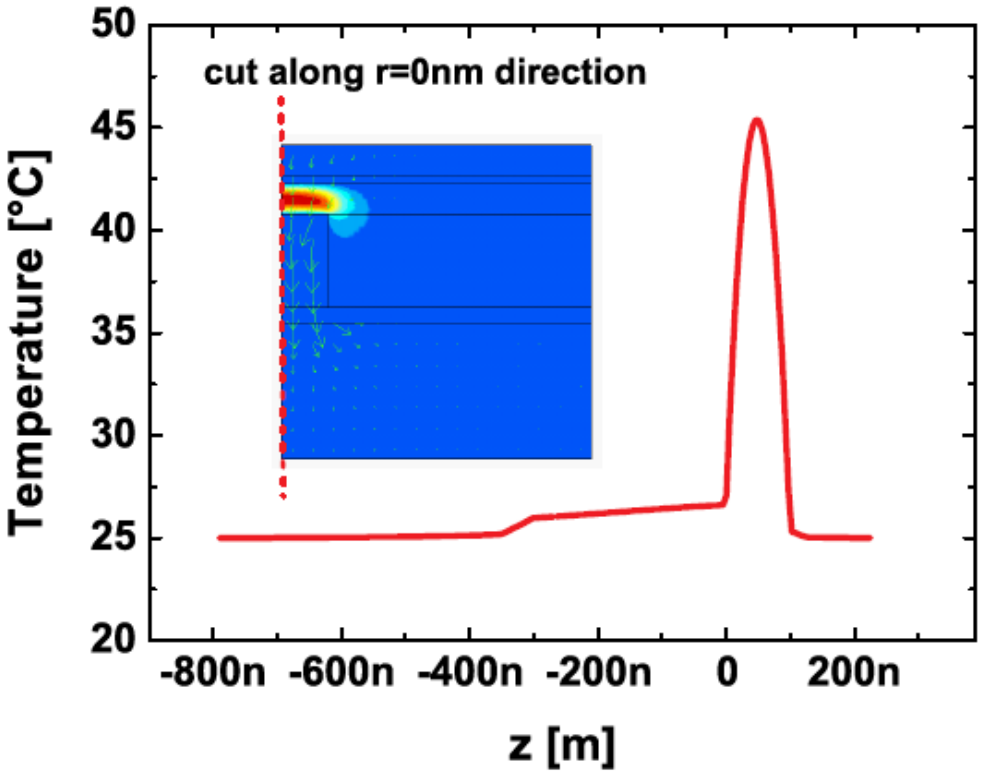

Figure 4.8: 2D-axial simulation of the temperature profile calculated along the z axis (cut in the $r = 0$nm direction of the PCM device). Simulation conditions are the same of Figure 4.7. The T profile as a function of z has a parabolic shape with peak located in $z = l_{GST}/2$.

4.8 Numerical simulations vs. Compact model

The aim of this Section is to compare 2D-axial FEM simulations vs. compact electro-thermal modeling approach to solve the electro-thermal problem under analysis. To this purpose, we calculate the temperature peak (T_{max}) in the device applying the same 1D analytical methodology suggested in [Iel11] and [Rus09]. In the papers [Iel11] and [Rus09] indeed, it is proposed an analytical procedure to solve an analogous electro-thermal problem, in which, as in our case, a relatively high resistance layer is sandwiched between two metal electrodes, which act as heat sinks. Therefore, assuming heat flowing only along the z direction, we rewrite Eq.(4.7) as:

$$\frac{d^2T}{dz^2} = -\frac{\mathbf{J}\cdot\mathbf{E}}{\kappa_{th,GST}}. \tag{4.10}$$

Solution of Eq.(4.10) in the $0 < z < l_{GST}$ domain can be obtained by imposing the boundary conditions at the plug and the electrodes, i.e. $T(z=0) = T_{amb}$ and $T(z=l_{GST}) = T_{amb}$, where l_{GST} is the GST thickness, yielding:

$$T(z) = T_{amb} - \frac{\mathbf{J}\cdot\mathbf{E}}{\kappa_{th,GST}}\left(\frac{z^2}{2} - \frac{z\cdot l_{GST}}{2}\right). \tag{4.11}$$

Note that Eq.(4.11) predicts T as a function of z to have a parabolic shape. This is confirmed by our electro-thermal simulations, as shown in Figure 4.8. Thus, since the temperature peak in the device is located in the vertical center of GST, i.e. $T_{max} = T(z = l_{GST}/2)$, Eq.(4.11) can be rewritten as:

$$T_{max} = T_{amb} + \frac{\mathbf{J}\cdot\mathbf{E}}{8\kappa_{th,GST}}\cdot {l_{GST}}^2. \tag{4.12}$$

In order to get the compact expression of Eq.(4.12) we consider the density of heating power $\mathbf{J}\cdot\mathbf{E}$ to be constant along z, which, obviously, is a quite rough physical approximation. Then, assuming heating effects occurring in a cylinder of radius equal to the radius of the heater, r_h =150nm, we get:

$$\mathbf{J}\cdot\mathbf{E} = \frac{V\cdot I}{\pi\cdot {r_h}^2\cdot l_{GST}}. \tag{4.13}$$

Finally, substituting Eq.(4.13) in Eq.(4.12), and by using $\kappa_{th,GST}$ = 0.3 W/(m·K), T_{amb} = 25°C, $V = V^*$ =183.2 mV and $I = I^*$=330.8 μA (being I^* the current experimental value corresponding to the V^* defined in Figure 4.6), we obtain $T_{max} \sim 60$°C. With the same physical parameters, 2D-axial simulation gives $T_{max} \sim 45$°C. Thus, the analytical approach provides a T_{max} significantly higher compared to the one

calculated by 2D-axial simulations, leading to an overestimation of SJH. Then, since in analytical Spice-like SJH modeling T_{max} is usually the temperature parameter used to calculate the electrical conductivity, the overestimation of the maximum temperature leads to the overestimation of GST electrical conductivity, and so of the current flowing through the device. For these reasons, we argue that classical Spice-like models, which, among the other assumptions discussed above, neglect also heating flux in the radial direction, are probably too approximated to obtain a correct estimation of Joule heating effects in the readout region of our polycrystalline PCM devices. To correctly apply this kind of methods in such a study, the introduction of suitable correction factors for the calculation of T_{max} are needed

4.9 Perspectives

Our results suggest that, to perform a robust modeling of SET-state PCM devices, physical mechanism(s) taking into account the electric field dependence of polycrystalline GST electrical conductivity must be identified. Recent advances on the comprehension of polycrystalline GST electronic and structural properties highlight indeed the "disordered" and complex nature of such a material, suggesting that its carrier transport physics might be regulated by disorder-induced mechanisms similar to the ones present in amorphous solids [Sie11], such as trap-assisted phenomena (e.g. Poole-Frenkel), and non-ohmic effects taking place at the electrodes (e.g. Schottky barriers and space-charge limited currents) [Mot71]. We think that grain-boundary limited conduction could be also worth investigating [Kam88]. In this framework, physical phenomena at the basis of this $I-V$ non-linearity must probably be studied by means of new experiments (e.g. cryogenic $I-V$ measurements) and through fabrication of novel device architectures.

4.10 Conclusions

In this work, we have investigated the impact of the Self-induced Joule-Heating (SJH) on the $I-V$ characteristics of polycrystalline GST-based PCM devices. We implemented an electro-thermal model, which has been solved by FEM simulations, and proposed a novel procedure (necessary condition test) to evaluate SJH. A comparative study between numerical simulations and analytical modeling has also been presented. The comparison between experimental data and simulations highlights that a model based on Ohm's law and SJH is not sufficiently accurate to capture the real physics of the device. To conclude, our work can be considered a further step towards the physical

comprehension of $I-V$ characteristics of SET state GST-based PCM devices, claiming for new experiments and theoretical efforts to investigate the electric field effects affecting polycrystalline GST carrier transport.

4.11 Acknowledgments

Thanks to Stefania Braga, Alessio Spessot, Paolo Fantini, and Andrea Ghetti for fruitful discussions and comments.

Conclusions

Investigation of electrical properties of Phase-Change Memory (PCM) devices has been at the heart of this Ph.D. thesis. In the following, a brief summary concerning the specific subjects, findings, and perspectives, of the research activity is provided.

In Chapter 2 we have presented, for the first time, a characterization study of carbon-doped GeTe (GeTeC) as promising candidate for next-generation PCM devices. We have shown that C doping leads to very good data retention performances: PCM cells integrating GeTeC10% can guarantee a 10 years fail temperature of about 127°C, compared to the 85°C of standard GST material. Furthermore, C doping reduces also fail time dispersion. Then, importantly, our analysis has pointed out the reduction of both RESET current and power for increasing carbon content. In particular, GeTeC10% PCM devices yield about a 30% of RESET current reduction in comparison to GST and GeTe ones, corresponding to about 50% of RESET power decrease. Programming time and resistance window of GeTeC devices are comparable to those of GST. For its outstanding properties of data retention and current/power consumption, GeTeC can be considered an ideal candidate to mitigate two of the main issues of today's PCM technology, namely reliability at high temperatures (to address the embedded-memory market specifications) and RESET current magnitude (governing selector area requirements, and so area occupation and cost).
Further research activities on this subject could include: i) GeTeC doping engineering for engineering performances (e.g. find the best trade off between data retention, RESET current and SET speed depending on the application) ii) ab-initio simulations for comprehension of the phenomena which stay at the origin of the GeTeC nature, and that can get more general information on the doping of phase-change materials.

Chapter 3 has been devoted to the implementation, characterization and modeling of an experimental setup for low-frequency noise measurements on two-terminals semiconductor devices. We have developed an analytical model to de-embed the setup-intrinsic noise contribution from the experimental measurements, enabling a reliable characterization of very-low noisy devices as well. Our equipment reproduces noise data on resistors, diodes and PCM in accordance with theory and recent literature. Moreover, the characterization of the *EG&G 5182* Low-Noise Amplifier (LNA) used in the setup has highlighted, for the first time, that when the resistance of the device under test stays within some specific ranges, the LNA behaves non-linearly (i.e. resonance effects arise), thus leading to measurement errors.
As a future research work, it would be very interesting to carry out a comparative study of noise behavior of the most promising phase-change materials. So far, the only low-frequency noise characterization published in literature is about GST. Since the normalized noise power increases with scaling, in the future low-frequency will probably be a "hot" research topic in the field of PCM.

In Chapter 4, we have studied the impact of Self-induced Joule-Heating (SJH) effect on the $I-V$ characteristics of fcc polycrystalline-GST PCM cells in the memory readout region. The investigation has been carried out by means of electrical characterization and electro-thermal simulations. Usually, the polycrystalline GST is considered as a simple resistor which electrical conductivity depends only on temperature. However, in our work, we have demonstrated that the effect of SJH is not sufficient to justify the non-linear shape of the $I-V$ characteristics. To derive a more reliable physical model, the electrical conductivity dependence on electric field must be studied.
This thesis work claims for a careful physical investigation of field effect in the SET-state transport properties.

Riassunto in lingua Italiana

La tesi di dottorato di Giovanni Betti Beneventi verte sulla caratterizzazione elettrica e la modellizzazione fisica di dispositivi di memoria non-volatile a cambiamento di fase. Questa tesi è stata effettuata nell'ambito di una co-tutela con l'Institut Polytechnique de Grenoble (Francia).

Il manoscritto in lingua inglese è costituito da quattro capitoli preceduti da un'introduzione e seguiti da una conclusione generale.

Il primo capitolo presenta un riassunto dello stato dell'arte delle memorie a cambiamento di fase. Inizialmente sono descritti i fenomeni principali governanti la fisica di questi dispositivi innovativi. In seguito sono discussi i vantaggi rispetto alle tradizionali memorie Flash, gli attuali punti deboli e le prospettive future di questa nuova tecnologia.

Il secondo capitolo è dedicato ai risultati di caratterizzazione materiale ed elettrica ottenuti su deposizioni blanket e su dispositivi di memoria a cambiamento di fase (PCM) basati sul nuovo materiale GeTe drogato carbonio (GeTeC), integrato al CEA-LETI (Francia) per al prima volta in assoluto nell'ambito di questo progetto di tesi. Il lavoro effettuato ha dimostrato che i dispositivi PCM basati sul GeTeC presentano delle caratteristiche molto interessanti: si è dimostrato in particolare un importante miglioramento della ritenzione del dato dalle alte temperature e una forte diminuzione della corrente di scrittura rispetto ai materiali calcogenuri attualmente utilizzati nell'industria delle memorie.

Il terzo capitolo descrive l'implementazione e la caratterizzazione sperimentale del setup per misure di rumore a bassa frequenza su dispositivi elettronici a due terminali sviluppato ai laboratori dell'Università di Modena e Reggio Emilia. Il rumore intrinseco alla catena di misura è stato caratterizzato e modellizzato analiticamente. Il modello ideato è stato rigorosamente validato caratterizzando il rumore di resistori, diodi e PCM.

Infine, nell'ultimo capitolo viene presentata un'analisi rigorosa avente come oggetto la valutazione dell'effetto di auto-riscaldamento Joule nella caratteristica I-V di dispositivi

di memoria a cambiamento di fase integranti il materiale $Ge_2Sb_2Te_5$ (il più utilizzato e conosciuto a livello mondiale per questo tipo di applicazioni) nella fase policristallina (livello logico 1 della memoria). La caratterizzazione sperimentale e le simulazioni elettrotermiche di strutture fabbricate ad-hoc per questo tipo di studio hanno permesso di valutare l'entità di un fenomeno lungamente dibattuto dagli specialisti di PCM. I risultati del lavoro mostrano molto chiaramente che l'auto-riscaldamento Joule non è sufficiente per rendere conto della non-linearità della caratteristica I-V dei dispositivi in esame.

Resumé en langue Française

La thèse de Giovanni Betti Beneventi portes sur la caractérisation électrique et la modélisation physique de dispositifs de mémoire non-volatile à changement de phase. Cette thèse a été effectuée dans le cadre d'une co-tutelle avec l'Università degli Studi di Modena e Reggio Emilia (Italie).
Le manuscrit en anglais comporte quatre chapitres précédés d'une introduction et terminés par une conclusion générale.
Le premier chapitre présent un résumé concernant l'état de l'art des mémoires a changement de phase. Initialement, les aspects principaux qui gouvernent la physique de ces dispositifs innovants sont décrits. Ensuite, les avantages par rapport aux traditionnels mémoires Flash, les défis actuels et les perspectives futures de cette technologie sont discutés.
Le deuxième chapitre est consacré aux résultats de caractérisation matériau et électrique obtenus sur déposition blanket et dispositifs de mémoire à changement de phase (PCM) basées sur le nouveau matériau GeTe dopé carbone (GeTeC), intégrés au LETI pour la première fois en absolu pendant ce travail de thèse. Les PCM basées sur le GeTeC montrent des performances très intéressant: on a démontré une importante amélioration de la rétention des donnes aux hautes températures et une forte diminution du courant d'écriture par rapport aux matériaux chalcogénures actuellement utilisées dans l'industrie de mémoires.
Le chapitre trois s'intéresse à l'implémentation et à la caractérisation expérimentale d'un setup de mesure de bruit a basse fréquence sur dispositifs électroniques a deux terminaux développé aux laboratoires de l'Università degli Studi di Modena e Reggio Emilia en Italie. Le bruit intrinsèque à la chaine de mesure a été caractérisé e modélisé analytiquement. Le modèle développé a été validé d'une manière robuste en caractérisant le bruit de résisteurs, diodes et de PCM.
Enfin, dans le dernier chapitre est présentée une analyse rigoureuse de l'effet d'auto-

chauffage Joule sur la caractéristique I-V des mémoires a changement de phase intégrant le matériau $Ge_2Sb_2Te_5$ (le plus utilisé et connu au niveau mondiale pour ce type d'application) dans la phase polycristalline (niveau logique 1 de la mémoire). La caractérisation expérimental ainsi que la simulation électrothermique des structures réalisé ad-hoc pour cette type de recherche on permit d'évaluer un phénomène longuement débattue par les spécialistes de PCM. Les résultats du travail montre d'une façon très claire que l'autochauffage Joule n'est pas suffisant pour explique la non-linéarité de la caractéristique I-V des dispositifs

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